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PROJECT INFORMATION

PHASE: SVT (Ver:1.0) 2019/07/05
BOM: 0.1
SVID: 17AA
SSID: 3178

BOM DISTRIBUTION RULE

QT, SMB&Consumer, Think M720e
(BOM, BOM, BOM)

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961	962	963	964	965	966	967	968
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977	978	979	980	981	982	983	984
985	986	987	988	989	990	991	992
993	994	995	996	997	998	999	1000

PCB Fab Note

Layer	Layer Name	Min/Typical/Max Layer Thickness (mil)	Dielectric Constant	Remark
L1	Solder Mask	0.4 / 0.65 / 1.8	3.40	
	Signal	1.4 / 1.90 / 2.4	NA	1.5 oz. (With Plating)
	Prepreg	2.2 / 2.75 / 3.2	3.90	
L2	Power/Gnd	1.0 / 1.20 / 1.4	NA	1. oz.
	Core	NA / 49.0 / NA	4.125	
L3	Power/Gnd	1.0 / 1.20 / 1.4	NA	1. oz.
	Prepreg	2.2 / 2.75 / 3.2	3.90	
L4	Signal	1.4 / 1.90 / 2.4	NA	1.5 oz. (With Plating)
	Solder Mask	0.4 / 0.65 / 1.8	3.40	

PCB / SILKSCREEN COLOR

PHASE	PCB	SILKSCREEN
ET	RED	YELLOW
SDV	Blue	WHITE
SIT/SIT-R/SVT	GREEN	WHITE

BOM DEFINITION:

MARKING	DESCRIPTION
I	INSTALL
NI	NOT INSTALL
MP	PRODUCTION PART ONLY
PROTO	NOT FOR PRODUCTION PART
CCL	CRITICAL COMPONENT LIST

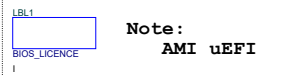
PCB Color and version:

ET phase:Red, V0.1
SDV phase:blue, V0.2
SIT phase:Green, V0.3
SVT and SS phase: Green,V1.0
after SS: Green, V1.x or VX.0

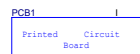
PCB Layer stack-up design:

The PCB total thickness must be within 1.6+/-0.13mm for DT chipset
The PCB total thickness must be within 1.2+/-0.10mm for Mobile chipset
The advised thickness of inner layer is within 1.2+/-10%mil.

BIOS Licence Label



PCB For CFL BIDDING BOX

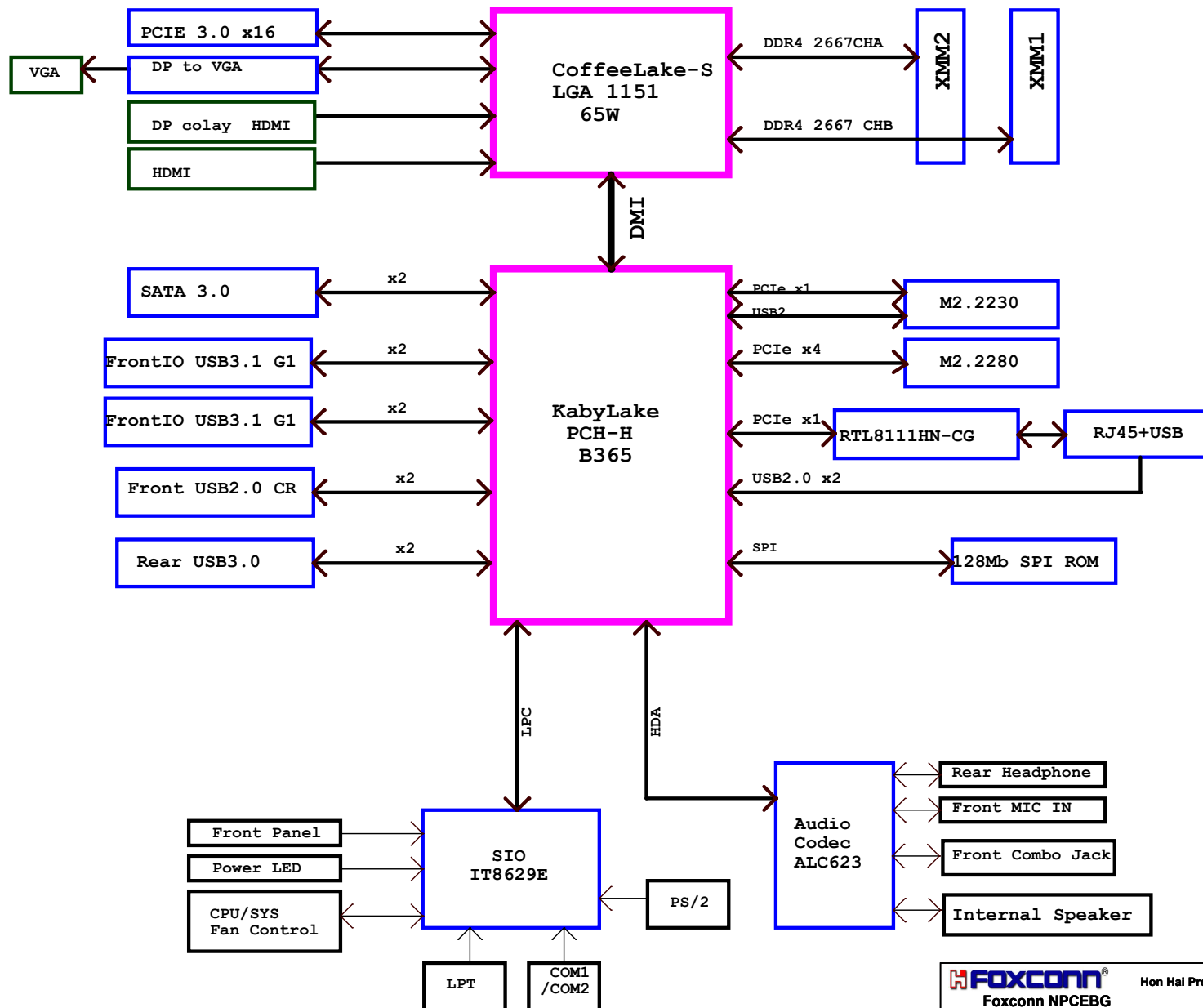


PCB B365_SVT_PCB
CFL-P
4-Layer PCB, Color With Green Soldermask, White Silkscreen, 11.14X7.87inch, CM-1, KB-6160, Rev.V1.0, ROHS
0101HGH01-491-G
GBM

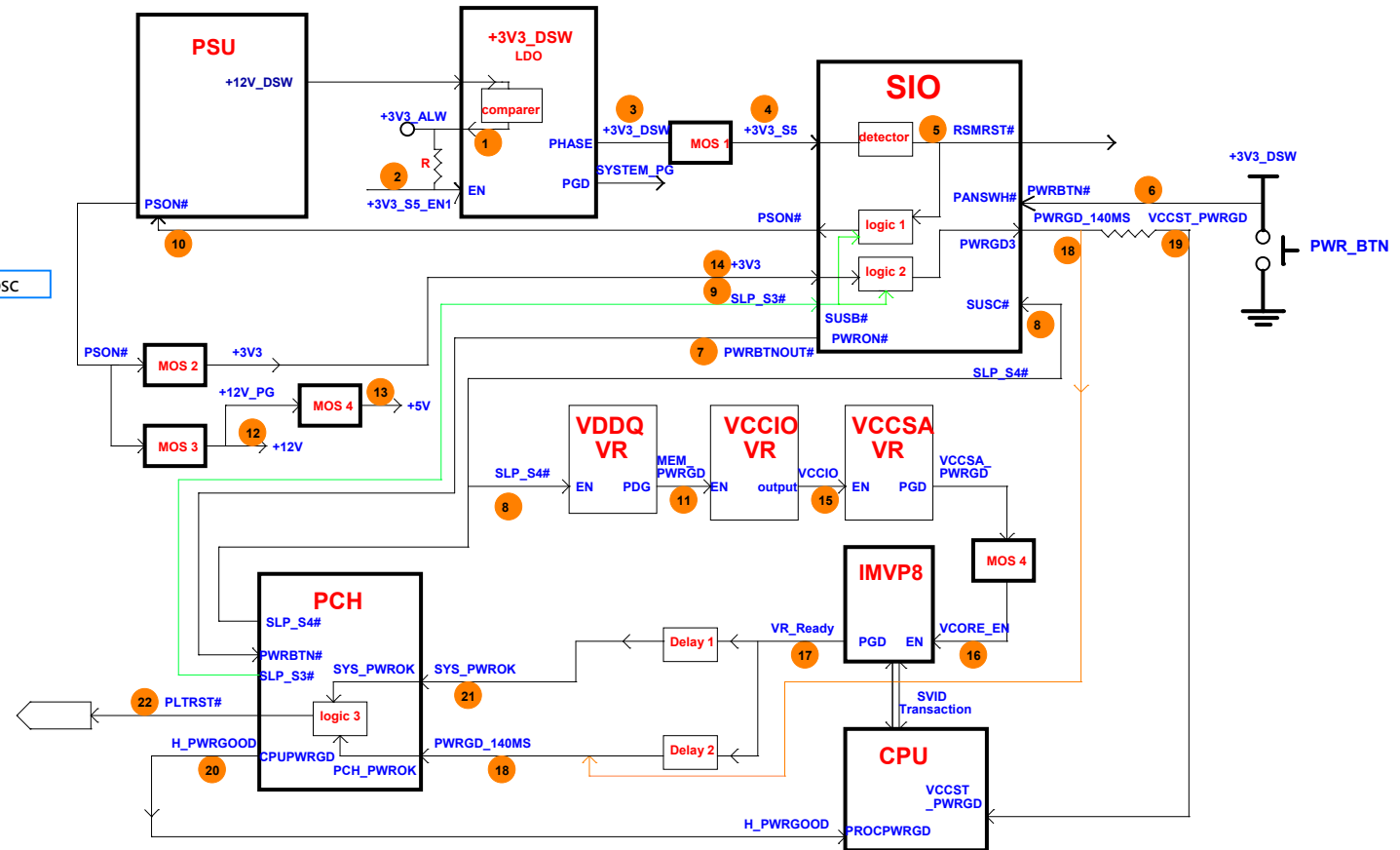
SVT

Part No.	Description	Supplier	Supplier P/N
0101HGH01-491-G	4-Layer PCB Color With Green Soldermask/White Silkscreen, 11.14X7.87 inch, CM-1, KB-6160, Rev.V1.0, ROHS	GBM	0101HGH01-491-G
0101HGH01-575-G	4-Layer PCB Color With Green Soldermask/White Silkscreen, 11.14X7.87 inch, ML-1, JT-150TC, Rev.V1.0, ROHS	FR	0101HGH01-575-G
0101HGH01-145-G	4-Layer PCB Color With Green Soldermask/White Silkscreen, 11.14X7.87 inch, GE-1, NP-140TL, Rev.V1.0, ROHS	ECS	0101HGH01-145-G

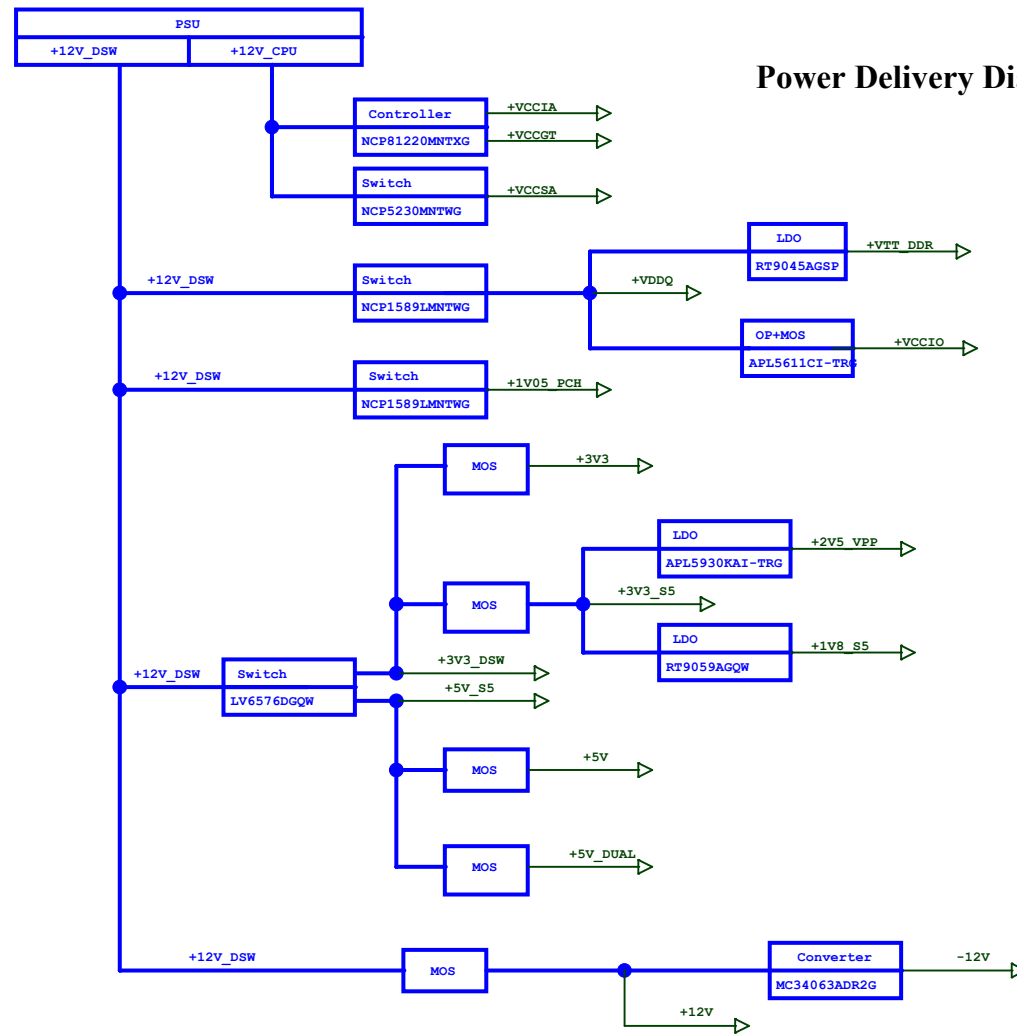
System BLOCK Diagram



RESET & POWER GOOD DIAGRAM



Power Delivery Diagram



CPU		
+VCCIA	VCCIA	79A
+VCCGT	VCCGT	45A
+VCCSA	VCCSA	11.1A
+VCCIO	VCCIO	6.4A
+VDDQ	VDDQ	3.3A
+VDDQ	VCCPLL_OC	0.13A
+1V0_S5	VCCST	0.08A
+1V0_S5	VCCPLL	0.15A

PCH		
+1V0_S5	VCC1P05V	10.936A
+3V3_S5	VCC3P3	2.519A
+3V3_DSW	VCCDSW	0.113A
+3V_BATT	VCCRTC	0.6mA

SIO		
+3V3_DSW	3VSB	0.02A
+3V3	AVCC3	0.02A
+3V_BATT	VCCBT	0.01A
+3V_BATT	VBAT	1uA

Audio Codec		
+3V3_S5	DVDD	0.04A
+3V3_S5	DVDD-IO	0.04A
+5V_S5	FVDD	1.22A

Realtek LAN		
+3V3_S5	DVDD33	0.065A
+3V3_S5	AVDD33	0.15A

DP2VGA		
+3V3	IVDD33	254mA
+3V3	OVDD33	1.6mA

PCIE x16		
+12V	3A	
+3V3	3A	
+3V3_S5	0.375A	

PCIE x1		
+12V	0.5A	
+3V3	3A	
+3V3_S5	0.375A	

M.2 2280		
+3V3	2A	

USB 2.0		
+5V_S5	0.5A	

USB 3.0		
+5V_S5	0.9A	

FAN		
+12V	0.6A	

DDR4		
+VTT_DDR	VDDQ	10.8A
+2V5_VPP	VPP	2.24A
+VTT_DDR	VTT	1A

[illegible][illegible]

PCH GPIO Table & Strap

[illegible][illegible]

	Order Part	Requisition code	Definition	MS in MS	Group Function	Location
OPF 10	OPF 10	OPF 10	OPF	MS	MS	MS
OPF 11	OPF 11	OPF 11	OPF	MS	MS	MS
OPF 12	OPF 12	OPF 12	OPF	MS	MS	MS
OPF 13	OPF 13	OPF 13	OPF	MS	MS	MS
OPF 14	OPF 14	OPF 14	OPF	MS	MS	MS
OPF 15	OPF 15	OPF 15	OPF	MS	MS	MS
OPF 16	OPF 16	OPF 16	OPF	MS	MS	MS
OPF 17	OPF 17	OPF 17	OPF	MS	MS	MS
OPF 18	OPF 18	OPF 18	OPF	MS	MS	MS
OPF 19	OPF 19	OPF 19	OPF	MS	MS	MS
OPF 20	OPF 20	OPF 20	OPF	MS	MS	MS
OPF 21	OPF 21	OPF 21	OPF	MS	MS	MS
OPF 22	OPF 22	OPF 22	OPF	MS	MS	MS
OPF 23	OPF 23	OPF 23	OPF	MS	MS	MS
OPF 24	OPF 24	OPF 24	OPF	MS	MS	MS
OPF 25	OPF 25	OPF 25	OPF	MS	MS	MS
OPF 26	OPF 26	OPF 26	OPF	MS	MS	MS
OPF 27	OPF 27	OPF 27	OPF	MS	MS	MS
OPF 28	OPF 28	OPF 28	OPF	MS	MS	MS
OPF 29	OPF 29	OPF 29	OPF	MS	MS	MS
OPF 30	OPF 30	OPF 30	OPF	MS	MS	MS
OPF 31	OPF 31	OPF 31	OPF	MS	MS	MS
OPF 32	OPF 32	OPF 32	OPF	MS	MS	MS
OPF 33	OPF 33	OPF 33	OPF	MS	MS	MS
OPF 34	OPF 34	OPF 34	OPF	MS	MS	MS
OPF 35	OPF 35	OPF 35	OPF	MS	MS	MS
OPF 36	OPF 36	OPF 36	OPF	MS	MS	MS
OPF 37	OPF 37	OPF 37	OPF	MS	MS	MS
OPF 38	OPF 38	OPF 38	OPF	MS	MS	MS
OPF 39	OPF 39	OPF 39	OPF	MS	MS	MS
OPF 40	OPF 40	OPF 40	OPF	MS	MS	MS
OPF 41	OPF 41	OPF 41	OPF	MS	MS	MS
OPF 42	OPF 42	OPF 42	OPF	MS	MS	MS
OPF 43	OPF 43	OPF 43	OPF	MS	MS	MS
OPF 44	OPF 44	OPF 44	OPF	MS	MS	MS
OPF 45	OPF 45	OPF 45	OPF	MS	MS	MS
OPF 46	OPF 46	OPF 46	OPF	MS	MS	MS
OPF 47	OPF 47	OPF 47	OPF	MS	MS	MS
OPF 48	OPF 48	OPF 48	OPF	MS	MS	MS
OPF 49	OPF 49	OPF 49	OPF	MS	MS	MS
OPF 50	OPF 50	OPF 50	OPF	MS	MS	MS
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OPF 90	OPF 90	OPF 90	OPF	MS	MS	MS
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OPF 96	OPF 96	OPF 96	OPF	MS	MS	MS
OPF 97	OPF 97	OPF 97	OPF	MS	MS	MS
OPF 98	OPF 98	OPF 98	OPF	MS	MS	MS
OPF 99	OPF 99	OPF 99	OPF	MS	MS	MS
OPF 100	OPF 100	OPF 100	OPF	MS	MS	MS

Signal	Usage	When Sampled	Comment
GPIO_R14 / SPI2	Top Speed Override	Sampling edge of PC1_PMODE	The signal has a weak internal pull-down. 0 = Disable strap speed override. (Default) 1 = Enable "Top Speed" mode
GPIO_R15 / SPI2F10Z	No Action	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Disable any lockdown mode. (Default) 1 = Enable any lockdown mode. (Default)
GPIO_C2 / SMCALREADY	TTL Compatibility	Sampling edge of SMCSTRB	When signal has a weak internal pull-down. 0 = Disable internal SMC Crypto Transport Layer Security (TLS) cipher suite (if implemented). (Default) 1 = Enable TLS SMC Crypto Transport Layer Security (TLS) cipher suite (if implemented)
GPIO_R12 / SPI2F10Z	Serial BIOS Boot	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. This signal controls the internal flow of access to the BIOS. When signal is sampled, the BIOS will start BIOS Deviation but (Host, Device), Functions, offset BCB, bit 61. 0 = SPI BIOS Deviation 1 = LSP BIOS Deviation
GPIO_C5 / SMCALREADY	Serial or LSP	Sampling edge of SMCSTRB	This signal has a weak internal pull-down. 0 = Serial (Default) 1 = LSP is selected (if required)
SPI0_M0Z1	Reserved	Sampling edge of SMCSTRB	External pull-up is required. Recommended 100K if pulled up to 3.3V or 1.8V if pulled up to 1.8V. This strap should sample SPI0. There should NOT be any on-board device driving its opposite direction during strap sampling
GPIO_R13 / SMCALREADY	Reserved	Sampling edge of SMCSTRB	External pull-up is required. Recommended 100K if pulled up to 3.3V or 1.8V if pulled up to 1.8V. This strap should sample SPI0. There should NOT be any on-board device driving its opposite direction during strap sampling
GPIO_R23 / SMCALREADY	Intel GCI-OOB	Sampling edge of SMCSTRB	External pull-up is required. Recommended 100K if pulled up to 3.3V or 1.8V if pulled up to 1.8V. This strap should sample SPI0. There should NOT be any on-board device driving its opposite direction during strap sampling
SPI0_I02	Reserved	Sampling edge of SMCSTRB	External pull-up is required. Recommended 100K if pulled up to 3.3V or 1.8V if pulled up to 1.8V. This strap should sample SPI0. There should NOT be any on-board device driving its opposite direction during strap sampling
SPI0_I03	Reserved	Sampling edge of SMCSTRB	External pull-up is required. Recommended 100K if pulled up to 3.3V or 1.8V if pulled up to 1.8V. This strap should sample SPI0. There should NOT be any on-board device driving its opposite direction during strap sampling
GPIO_R00 / I2C0_I2O	Flash Descriptor Override	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Disable I2C0. (Default) 1 = Enable I2C0. (Default)
GPIO_R22 / SMCALREADY	Flash Descriptor Override	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Disable Flash Descriptor Security (override 1). (Default) 1 = Enable Flash Descriptor Security (override 1)
GPIO_R24 / SMCALREADY	Flash Descriptor Override	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Master Attached Flash Sharing (MAFS) disabled
GPIO_C14 / GPIO_C15	Display Output C1 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 0 is not detected. (Default) 1 = Port 0 is detected. (Default)
GPIO_C16 / GPIO_C17	Display Output C2 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 1 is not detected. (Default) 1 = Port 1 is detected. (Default)
GPIO_C18 / GPIO_C19	Display Output C3 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 2 is not detected. (Default) 1 = Port 2 is detected. (Default)
GPIO_C20 / GPIO_C21 / GPIO_C22	Display Output C4 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 3 is not detected. (Default) 1 = Port 3 is detected. (Default)
GPIO_C23 / GPIO_C24 / GPIO_C25 / GPIO_C26	Display Output C5 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 4 is not detected. (Default) 1 = Port 4 is detected. (Default)
GPIO_C27 / GPIO_C28 / GPIO_C29 / GPIO_C30 / GPIO_C31 / GPIO_C32	Display Output C6 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 5 is not detected. (Default) 1 = Port 5 is detected. (Default)
GPIO_C33 / GPIO_C34 / GPIO_C35 / GPIO_C36 / GPIO_C37 / GPIO_C38 / GPIO_C39 / GPIO_C40 / GPIO_C41 / GPIO_C42	Display Output C7 Selected	Sampling edge of PC1_PMODE	This signal has a weak internal pull-down. 0 = Port 6 is not detected. (Default) 1 = Port 6 is detected. (Default)
GPIO_C43 / GPIO_C44 / GPIO_C45 / GPIO_C46 / GPIO_C47 / GPIO_C48 / GPIO_C49 / GPIO_C50 / GPIO_C51 / GPIO_C52 / GPIO_C53 / GPIO_C54 / GPIO_C55 / GPIO_C56 / GPIO_C57 / GPIO_C58 / GPIO_C59 / GPIO_C60 / GPIO_C61 / GPIO_C62 / GPIO_C63 / GPIO_C64 / GPIO_C65 / GPIO_C66 / GPIO_C67 / GPIO_C68 / GPIO_C69 / GPIO_C70 / GPIO_C71 / GPIO_C72 / GPIO_C73 / GPIO_C74 / GPIO_C75 / GPIO_C76 / GPIO_C77 / GPIO_C78 / GPIO_C79 / GPIO_C80 / GPIO_C81 / GPIO_C82 / GPIO_C83 / GPIO_C84 / GPIO_C85 / GPIO_C86 / GPIO_C87 / GPIO_C88 / GPIO_C89 / GPIO_C90 / GPIO_C91 / GPIO_C92 / GPIO_C93 / GPIO_C94 / GPIO_C95 / GPIO_C96 / GPIO_C97 / GPIO_C98 / GPIO_C99 / GPIO_C100 / GPIO_C101 / GPIO_C102 / GPIO_C103 / GPIO_C104 / GPIO_C105 / GPIO_C106 / GPIO_C107 / GPIO_C108 / GPIO_C109 / GPIO_C110 / GPIO_C111 / GPIO_C112 / GPIO_C113 / GPIO_C114 / GPIO_C115 / GPIO_C116 / GPIO_C117 / GPIO_C118 / GPIO_C119 / GPIO_C120 / GPIO_C121 / GPIO_C122 / GPIO_C123 / GPIO_C124 / GPIO_C125 / GPIO_C126 / GPIO_C127 / GPIO_C128 / GPIO_C129 / GPIO_C130 / GPIO_C131 / GPIO_C132 / GPIO_C133 / GPIO_C134 / GPIO_C135 / GPIO_C136 / GPIO_C137 / GPIO_C138 / GPIO_C139 / GPIO_C140 / GPIO_C141 / GPIO_C142 / GPIO_C143 / GPIO_C144 / GPIO_C145 / GPIO_C146 / GPIO_C147 / GPIO_C148 / GPIO_C149 / GPIO_C150 / GPIO_C151 / GPIO_C152 / GPIO_C153 / GPIO_C154 / GPIO_C155 / GPIO_C156 / GPIO_C157 / GPIO_C158 / GPIO_C159 / GPIO_C160 / GPIO_C161 / GPIO_C162 / GPIO_C163 / GPIO_C164 / GPIO_C165 / GPIO_C166 / GPIO_C167 / GPIO_C168 / GPIO_C169 / GPIO_C170 / GPIO_C171 / GPIO_C172 / GPIO_C173 / GPIO_C174 / GPIO_C175 / GPIO_C176 / GPIO_C177 / GPIO_C178 / GPIO_C179 / GPIO_C180 / GPIO_C181 / GPIO_C182 / GPIO_C183 / GPIO_C184 / GPIO_C185 / GPIO_C186 / GPIO_C187 / GPIO_C188 / GPIO_C189 / GPIO_C190 / GPIO_C191 / GPIO_C192 / GPIO_C193 / GPIO_C194 / GPIO_C195 / GPIO_C196 / GPIO_C197 / GPIO_C198 / GPIO_C199 / GPIO_C200 / GPIO_C201 / GPIO_C202 / GPIO_C203 / GPIO_C204 / GPIO_C205 / GPIO_C206 / GPIO_C207 / GPIO_C208 / GPIO_C209 / GPIO_C210 / GPIO_C211 / GPIO_C212 / GPIO_C213 / GPIO_C214 / GPIO_C215 / GPIO_C216 / GPIO_C217 / GPIO_C218 / GPIO_C219 / GPIO_C220 / GPIO_C221 / GPIO_C222 / GPIO_C223 / GPIO_C224 / GPIO_C225 / GPIO_C226 / GPIO_C227 / GPIO_C228 / GPIO_C229 / GPIO_C230 / GPIO_C231 / GPIO_C232 / GPIO_C233 / GPIO_C234 / GPIO_C235 / GPIO_C236 / GPIO_C237 / GPIO_C238 / GPIO_C239 / GPIO_C240 / GPIO_C241 / GPIO_C242 / GPIO_C243 / GPIO_C244 / GPIO_C245 / GPIO_C246 / GPIO_C247 / GPIO_C248 / GPIO_C249 / GPIO_C250 / GPIO_C251 / GPIO_C252 / GPIO_C253 / GPIO_C254 / GPIO_C255 / GPIO_C256 / GPIO_C257 / GPIO_C258 / GPIO_C259 / GPIO_C260 / GPIO_C261 / GPIO_C262 / GPIO_C263 / GPIO_C264 / GPIO_C265 / GPIO_C266 / GPIO_C267 / GPIO_C268 / GPIO_C269 / GPIO_C270 / GPIO_C271 / GPIO_C272 / GPIO_C273 / GPIO_C274 / GPIO_C275 / GPIO_C276 / GPIO_C277 / GPIO_C278 / GPIO_C279 / GPIO_C280 / GPIO_C281 / GPIO_C282 / GPIO_C283 / GPIO_C284 / GPIO_C285 / GPIO_C286 / GPIO_C287 / GPIO_C288 / GPIO_C289 / GPIO_C290 / GPIO_C291 / GPIO_C292 / GPIO_C293 / GPIO_C294 / GPIO_C295 / GPIO_C296 / GPIO_C297 / GPIO_C298 / GPIO_C299 / GPIO_C300 / GPIO_C301 / GPIO_C302 / GPIO_C303 / GPIO_C304 / GPIO_C305 / GPIO_C306 / GPIO_C307 / GPIO_C308 / GPIO_C309 / GPIO_C310 / GPIO_C311 / GPIO_C312 / GPIO_C313 / GPIO_C314 / GPIO_C315 / GPIO_C316 / GPIO_C317 / GPIO_C318 / GPIO_C319 / GPIO_C320 / GPIO_C321 / GPIO_C322 / GPIO_C323 / GPIO_C324 / GPIO_C325 / GPIO_C326 / GPIO_C327 / GPIO_C328 / GPIO_C329 / GPIO_C330 / GPIO_C331 / GPIO_C332 / GPIO_C333 / GPIO_C334 / GPIO_C335 / GPIO_C336 / GPIO_C337 / GPIO_C338 / GPIO_C339 / GPIO_C340 / GPIO_C341 / GPIO_C342 / GPIO_C343 / GPIO_C344 / GPIO_C345 / GPIO_C346 / GPIO_C347 / GPIO_C348 / GPIO_C349 / GPIO_C350 / GPIO_C351 / GPIO_C352 / GPIO_C353 / GPIO_C354 / GPIO_C355 / GPIO_C356 / GPIO_C357 / GPIO_C358 / GPIO_C359 / GPIO_C360 / GPIO_C361 / GPIO_C362 / GPIO_C363 / GPIO_C364 / GPIO_C365 / GPIO_C366 / GPIO_C367 / GPIO_C368 / GPIO_C369 / GPIO_C370 / GPIO_C371 / GPIO_C372 / GPIO_C373 / GPIO_C374 / GPIO_C375 / GPIO_C376 / GPIO_C377 / GPIO_C378 / GPIO_C379 / GPIO_C380 / GPIO_C381 / GPIO_C382 / GPIO_C383 / GPIO_C384 / GPIO_C385 / GPIO_C386 / GPIO_C387 / GPIO_C388 / GPIO_C389 / GPIO_C390 / GPIO_C391 / GPIO_C392 / GPIO_C393 / GPIO_C394 / GPIO_C395 / GPIO_C396 / GPIO_C397 / GPIO_C398 / GPIO_C399 / GPIO_C400 / GPIO_C401 / GPIO_C402 / GPIO_C403 / GPIO_C404 / GPIO_C405 / GPIO_C406 / GPIO_C407 / GPIO_C408 / GPIO_C409 / GPIO_C410 / GPIO_C411 / GPIO_C412 / GPIO_C413 / GPIO_C414 / GPIO_C415 / GPIO_C416 / GPIO_C417 / GPIO_C418 / GPIO_C419 / GPIO_C420			

Item Ref	Management area	Database	DB or MS	Group Number	Frequency
GPV 00	Management area	MS	MS	0000	1000000000
GPV 01	Management area	MS	MS	0000	1000000000
GPV 02	Management area	MS	MS	0000	1000000000
GPV 03	Management area	MS	MS	0000	1000000000
GPV 04	Management area	MS	MS	0000	1000000000
GPV 05	Management area	MS	MS	0000	1000000000
GPV 06	Management area	MS	MS	0000	1000000000
GPV 07	Management area	MS	MS	0000	1000000000
GPV 08	Management area	MS	MS	0000	1000000000
GPV 09	Management area	MS	MS	0000	1000000000
GPV 10	Management area	MS	MS	0000	1000000000
GPV 11	Management area	MS	MS	0000	1000000000
GPV 12	Management area	MS	MS	0000	1000000000
GPV 13	Management area	MS	MS	0000	1000000000
GPV 14	Management area	MS	MS	0000	1000000000
GPV 15	Management area	MS	MS	0000	1000000000
GPV 16	Management area	MS	MS	0000	1000000000
GPV 17	Management area	MS	MS	0000	1000000000
GPV 18	Management area	MS	MS	0000	1000000000
GPV 19	Management area	MS	MS	0000	1000000000
GPV 20	Management area	MS	MS	0000	1000000000
GPV 21	Management area	MS	MS	0000	1000000000
GPV 22	Management area	MS	MS	0000	1000000000
GPV 23	Management area	MS	MS	0000	1000000000

	Item No.	Designated with	Refers	W or M	Item Period	Amount
GRP F1	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F2	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F3	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F4	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F5	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F6	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F7	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F8	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F9	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F10	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F11	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F12	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F13	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F14	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F15	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F16	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F17	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F18	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F19	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F20	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F21	1000000000	1000000000	1000000000	W	1000	1000000000
GRP F22	1000000000	1000000000	1000000000	W	1000	1000000000

[illegible]

	Power Rail	Microprocessor Aids	Behavior	ECU via CAN	Engine Parameters	Transmission
00FF-03	00000000	00000000	00000000	0000	0000	00000000
00FF-04	00000000	00000000	00000000	0000	0000	00000000
00FF-05	00000000	00000000	00000000	0000	0000	00000000
00FF-06	00000000	00000000	00000000	0000	0000	00000000
00FF-07	00000000	00000000	00000000	0000	0000	00000000
00FF-08	00000000	00000000	00000000	0000	0000	00000000
00FF-09	00000000	00000000	00000000	0000	0000	00000000
00FF-0A	00000000	00000000	00000000	0000	0000	00000000
00FF-0B	00000000	00000000	00000000	0000	0000	00000000
00FF-0C	00000000	00000000	00000000	0000	0000	00000000
00FF-0D	00000000	00000000	00000000	0000	0000	00000000
00FF-0E	00000000	00000000	00000000	0000	0000	00000000
00FF-0F	00000000	00000000	00000000	0000	0000	00000000
00FF-10	00000000	00000000	00000000	0000	0000	00000000
00FF-11	00000000	00000000	00000000	0000	0000	00000000
00FF-12	00000000	00000000	00000000	0000	0000	00000000
00FF-13	00000000	00000000	00000000	0000	0000	00000000
00FF-14	00000000	00000000	00000000	0000	0000	00000000
00FF-15	00000000	00000000	00000000	0000	0000	00000000
00FF-16	00000000	00000000	00000000	0000	0000	00000000
00FF-17	00000000	00000000	00000000	0000	0000	00000000
00FF-18	00000000	00000000	00000000	0000	0000	00000000
00FF-19	00000000	00000000	00000000	0000	0000	00000000
00FF-1A	00000000	00000000	00000000	0000	0000	00000000
00FF-1B	00000000	00000000	00000000	0000	0000	00000000
00FF-1C	00000000	00000000	00000000	0000	0000	00000000
00FF-1D	00000000	00000000	00000000	0000	0000	00000000
00FF-1E	00000000	00000000	00000000	0000	0000	00000000
00FF-1F	00000000	00000000	00000000	0000	0000	00000000

	Power Unit	Religiosity index	Defection	MS or MS	Strong Protestant	Protestant
GFF G0	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G1	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G2	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G3	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G4	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G5	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G6	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20
GFF G7	Protestant 1971 = 35.360		(.25)	MS	Protest	MS 20

	Power Plant	Recapitalized units	Debtless	2001 or 2002	Group Transition	Comments
OFF E0	Operating	None	None	None	None	None
OFF E1	Operating	None	None	None	None	None
OFF E2	Operating	None	None	None	None	None
OFF E3	Operating	None	None	None	None	None
OFF E4	Operating	None	None	None	None	None
OFF E5	Operating	None	None	None	None	None
OFF E6	Operating	None	None	None	None	None
OFF E7	Operating	None	None	None	None	None
OFF E8	Operating	Operating	Operating	None	None	None
OFF E9	Operating	Operating	Operating	None	None	None
OFF E10	Operating	Operating	Operating	None	None	None
OFF E11	Operating	Operating	Operating	None	None	None
OFF E12	Operating	Operating	Operating	None	None	None
OFF E13	Operating	Operating	Operating	None	None	None
OFF E14	Operating	Operating	Operating	None	None	None
OFF E15	Operating	Operating	Operating	None	None	None
OFF E16	Operating	Operating	Operating	None	None	None
OFF E17	Operating	Operating	Operating	None	None	None
OFF E18	Operating	Operating	Operating	None	None	None
OFF E19	Operating	Operating	Operating	None	None	None
OFF E20	Operating	Operating	Operating	None	None	None
OFF E21	Operating	Operating	Operating	None	None	None
OFF E22	Operating	Operating	Operating	None	None	None
OFF E23	Operating	Operating	Operating	None	None	None

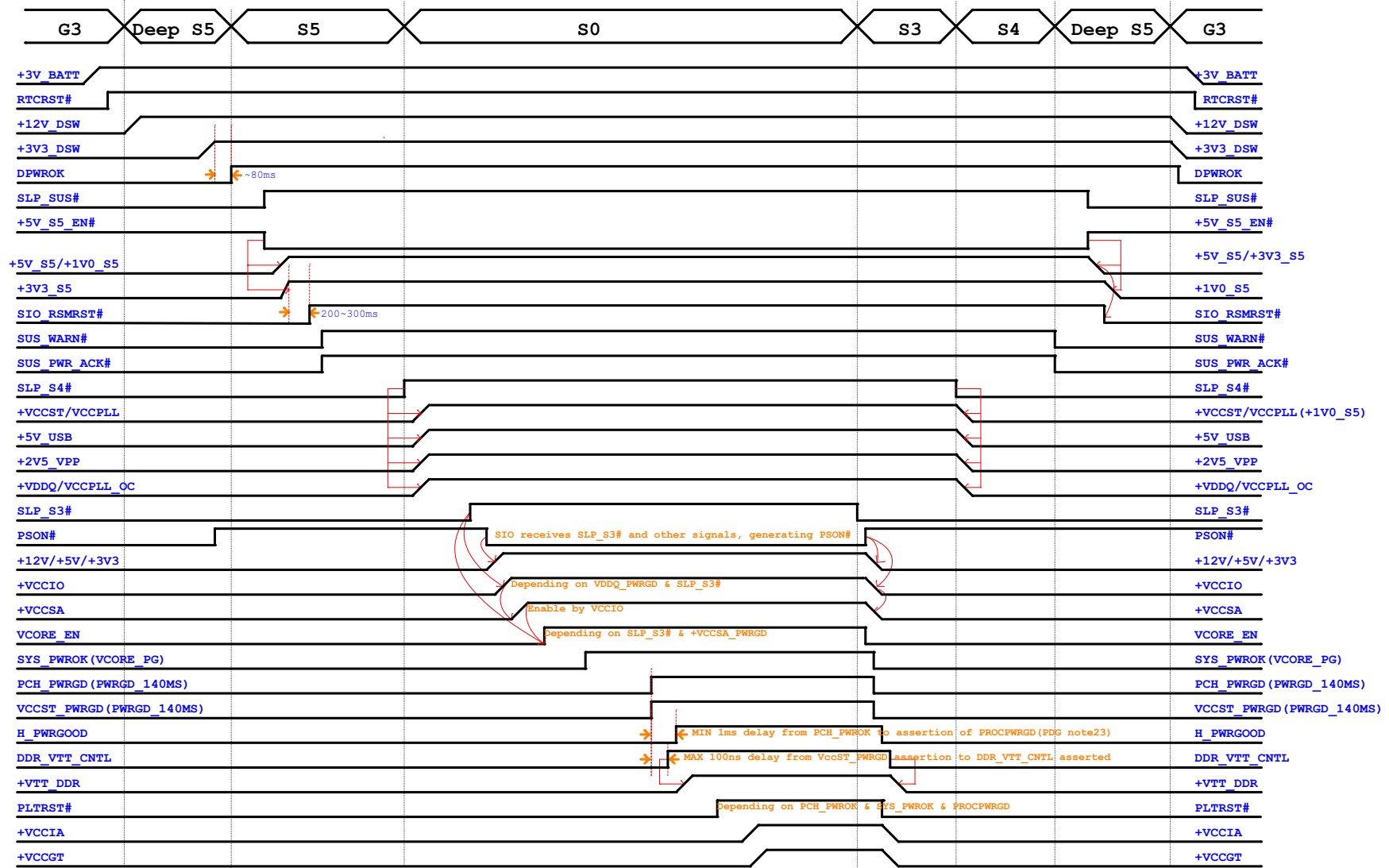
[illegible]

	Asset Type	Relationship with	Definition	SB in SB	Group Portfolio	Exclusion
COP 01	Investment	Investment	SB	SB	SB	SB
COP 01	Investment	Investment	SB	SB	SB	SB
COP 02	Investment	Investment	SB	SB	SB	SB
COP 03	Investment	Investment	SB	SB	SB	SB
COP 04	Investment	Investment	SB	SB	SB	SB
COP 05	Investment	Investment	SB	SB	SB	SB
COP 06	Investment	Investment	SB	SB	SB	SB
COP 07	Investment	Investment	SB	SB	SB	SB
COP 08	Investment	Investment	SB	SB	SB	SB
COP 09	Investment	Investment	SB	SB	SB	SB
COP 10	Investment	Investment	SB	SB	SB	SB
COP 11	Investment	Investment	SB	SB	SB	SB
COP 12	Investment	Investment	SB	SB	SB	SB
COP 13	Investment	Investment	SB	SB	SB	SB
COP 14	Investment	Investment	SB	SB	SB	SB
COP 15	Investment	Investment	SB	SB	SB	SB
COP 16	Investment	Investment	SB	SB	SB	SB
COP 17	Investment	Investment	SB	SB	SB	SB
COP 18	Investment	Investment	SB	SB	SB	SB
COP 19	Investment	Investment	SB	SB	SB	SB
COP 20	Investment	Investment	SB	SB	SB	SB
COP 21	Investment	Investment	SB	SB	SB	SB
COP 22	Investment	Investment	SB	SB	SB	SB
COP 23	Investment	Investment	SB	SB	SB	SB
COP 24	Investment	Investment	SB	SB	SB	SB
COP 25	Investment	Investment	SB	SB	SB	SB

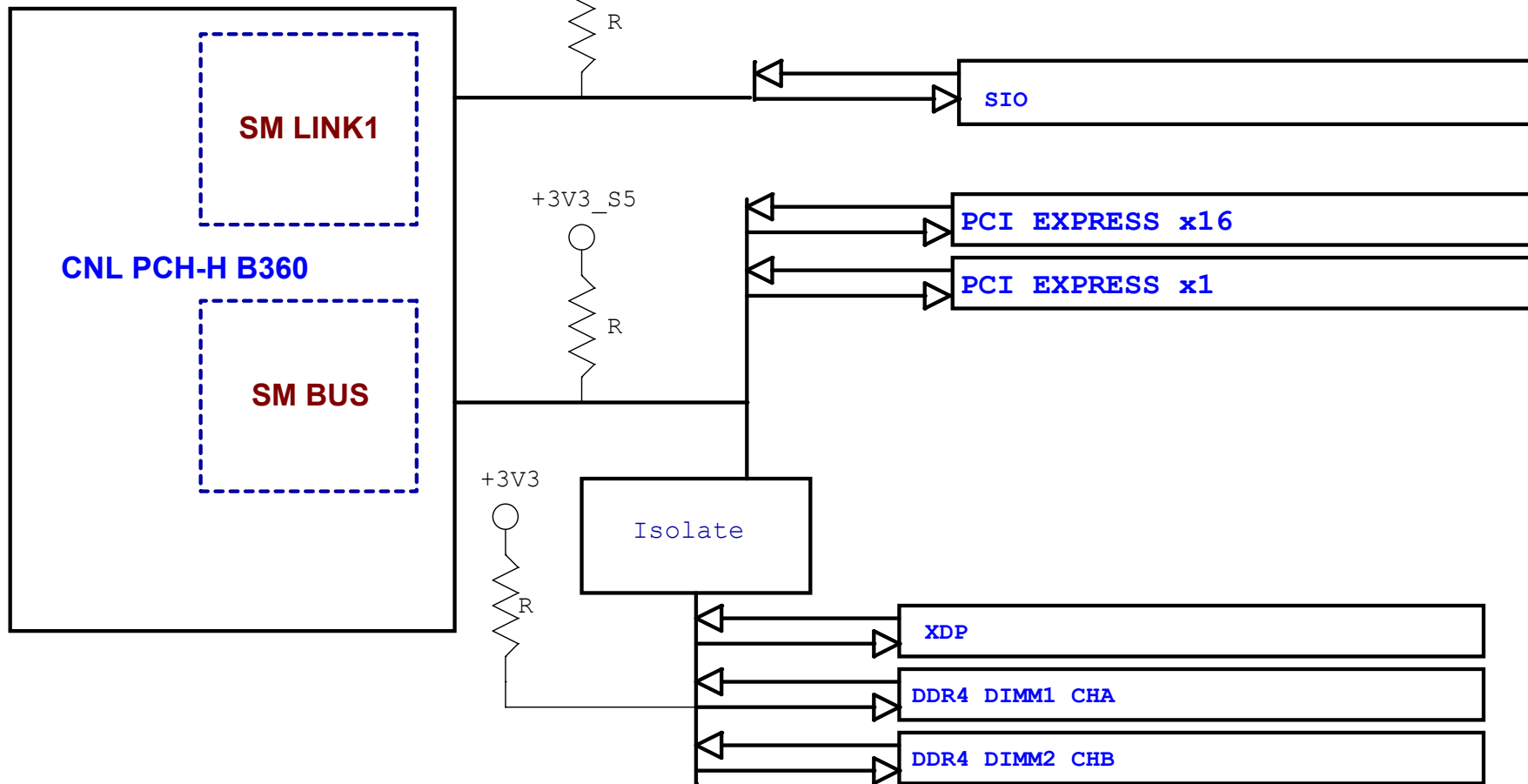
	From Date	Relationship with	Definition	DOI or SEC	Group Function	Function
CP00	1/1/2000	Customer	Customer			Act Head
CP01	1/1/2000	Customer	Customer	None		Act Head
CP02	1/1/2000	Customer	Customer	None		Act Head
CP03	1/1/2000	Customer	Customer	None		Act Head
CP04	1/1/2000	Customer	Customer	None		Act Head
CP05	1/1/2000	Customer	Customer	None		Act Head
CP06	1/1/2000	Customer	Customer	None		Act Head
CP07	1/1/2000	Customer	Customer	None		Act Head
CP08	1/1/2000	Customer	Customer	None		Act Head
CP09	1/1/2000	Customer	Customer	None		Act Head
CP10	1/1/2000	Customer	Customer	None		Act Head
CP11	1/1/2000	Customer	Customer	None		Act Head

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DEEP SLEEP POWER SEQUENCE DIAGRAM

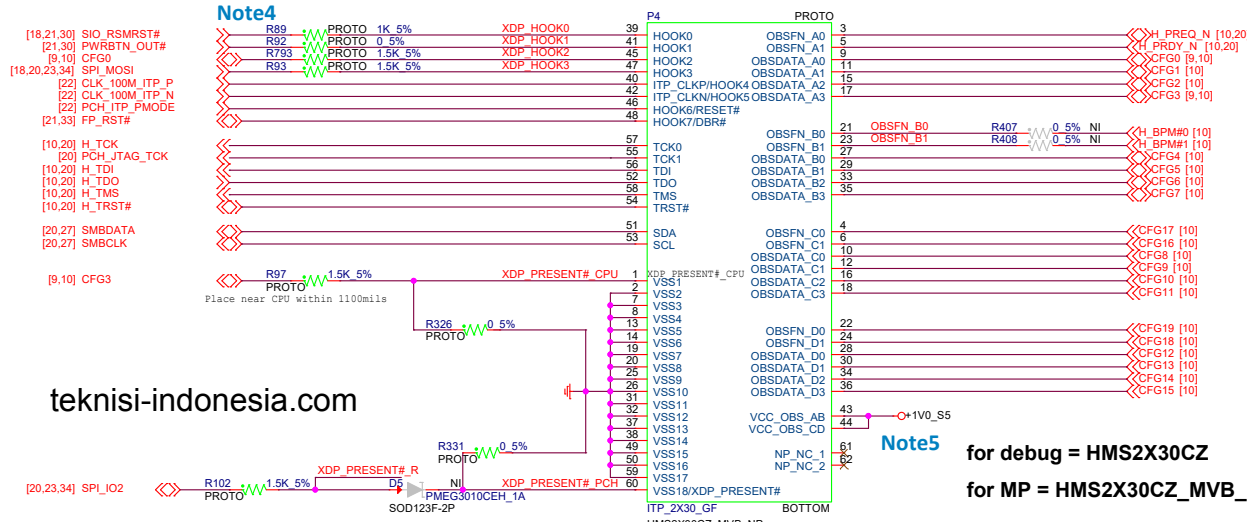


SMBUS DIAGRAM



Intel MCP XDP Debug Connector

PRDY# and PREQ# must connect for DCI Merged Debug Port Topology



Design Note

Note 1: XDP Connector Footprint

NPI
HMS2X30CZ
MVB
HMS2X30CZ_MVB_NP

Note 2

C74 Place close to P4 Connector
C75 Place close to P4 Connector
R792 Place close to P4 Connector
R86 Place close to P4 Connector
R87 Place close to P4 Connector
R796 Close P4

Note3

R891 Place Close to U4 Within 1.1"
R116 Place Close to U4 Within 1.1"
R235 Place Close to U4 Within 1.5"
R236 Place Close to U4 Within 1.5"
R371 Place Close to U4 Within 1.5"
C70 Place Close to R235, R236, R371

Note4

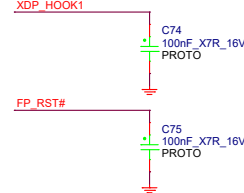
R793 Place close to T Point
R89 Place close to T Point
R102 Place close to Tpoint within 500mils (PCH_SPI_IO2)
R93 Close to T-Point of SPI_MOSI < 1100mils
R152 Place Close to CPU Within 1.5"
R117 Place Close to CPU Within 1.5"

Note5

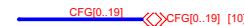
P4.43 and P4.44 Power trace width = 10mils

DeCoupling CAP

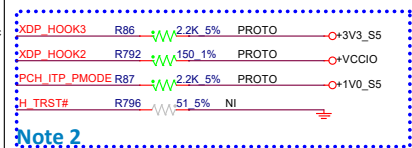
Note 2



CFG Connection

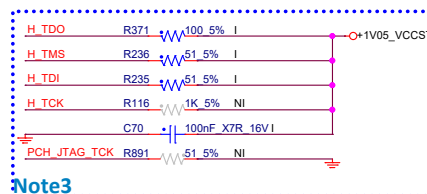


HW PU/PD Configuration



Note 2

Note 4



Note3

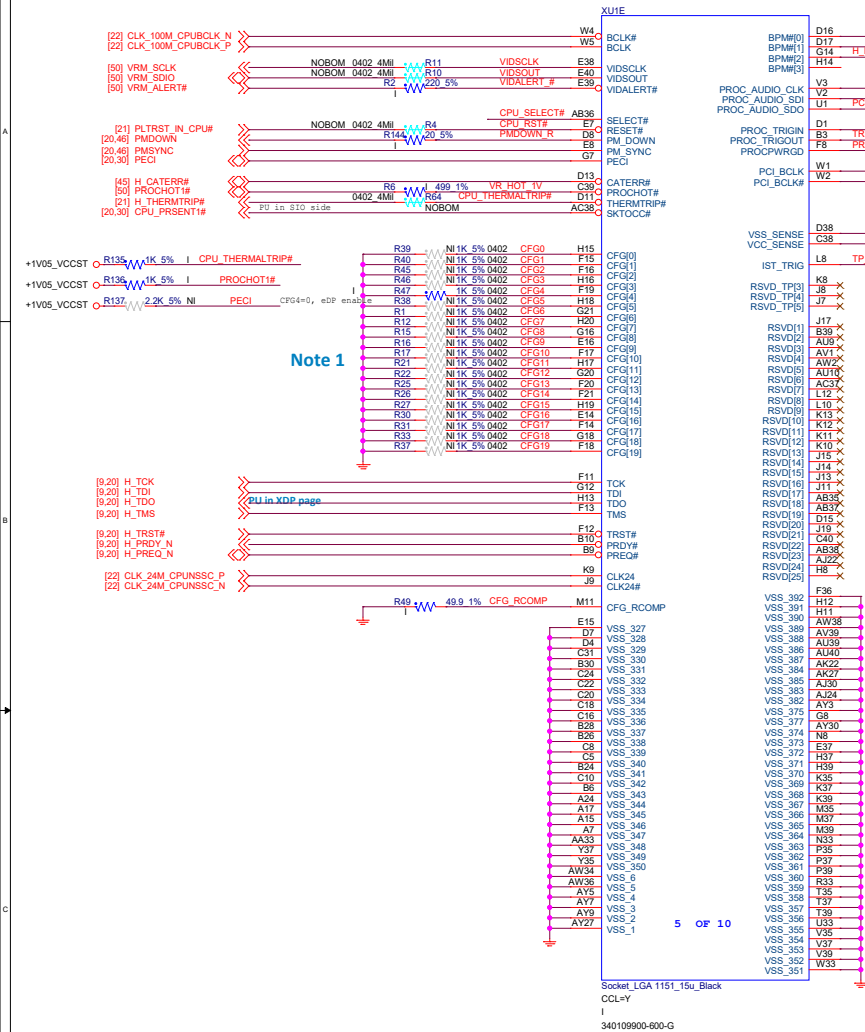
BOM Change list for MP PCA if need to enable DCI/XDP:

- 1.Remove P4 soldermask on pad and install P4 XDP connector.
- 2.Install D5,R86,R87,R89,R92,R93,R97,R102,R792,R793

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Title 09. CPU XDP			
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MCP- VRM/CLK/CTRL/JTAG

CPU - D part



Note 1

PEI-E CONFIG TABLE		
CFG6	CFG5	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

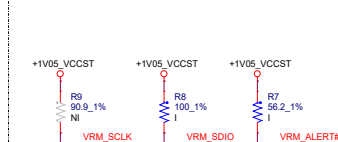
ALL PINS HAVE INTERNAL PULL-UPS

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1			RESERVED
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3			RESERVED
4	DISABLE	ENABLE "0"	eDP enable
5	ENABLE "1"	DISABLE "0"	PEG0CFGSEL[0] x16
6	ENABLE "1"	DISABLE "0"	PEG0CFGSEL[1] x16
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8-19			RESERVED

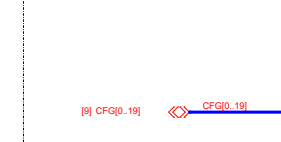
CPU Part E - HW PU/PD and Decoupling



VRM Pull-Up

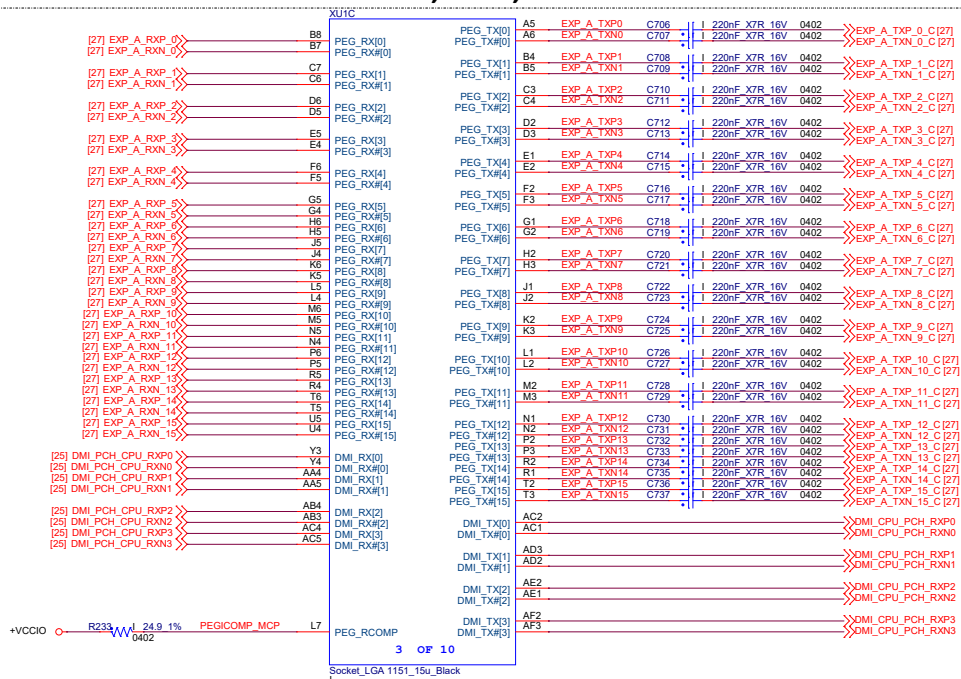
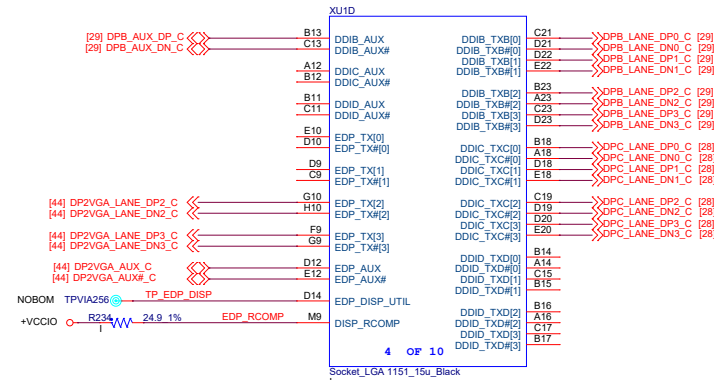


CFG Connection



CPU - A/B part
DDR Channel A/B

MCP - PEG, DMI, DDI

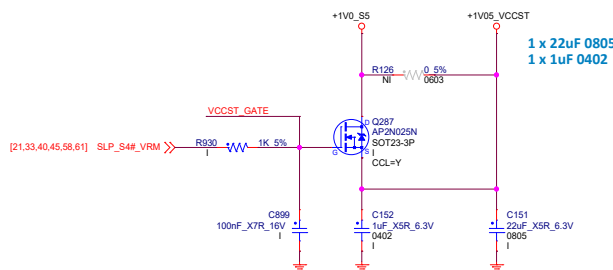
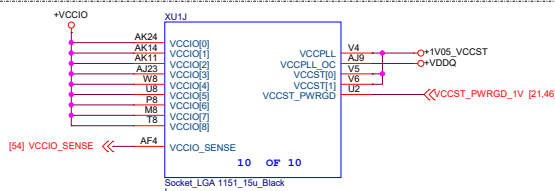
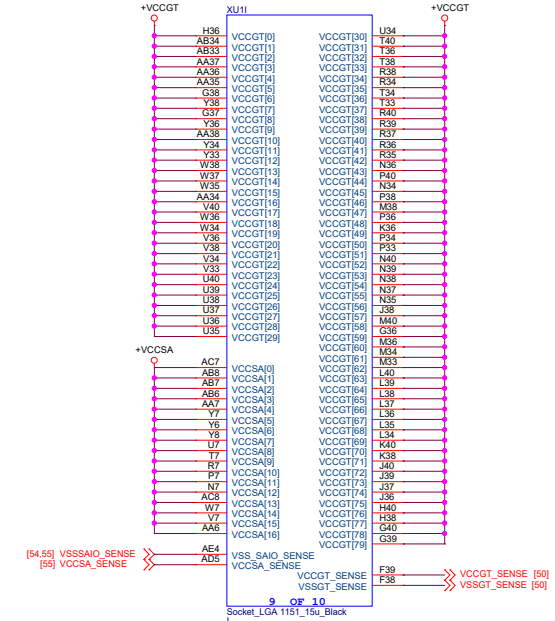
CPU - C part
PEG&DMICPU - D part
Displayport

MCP - POWER CONNECTIONS

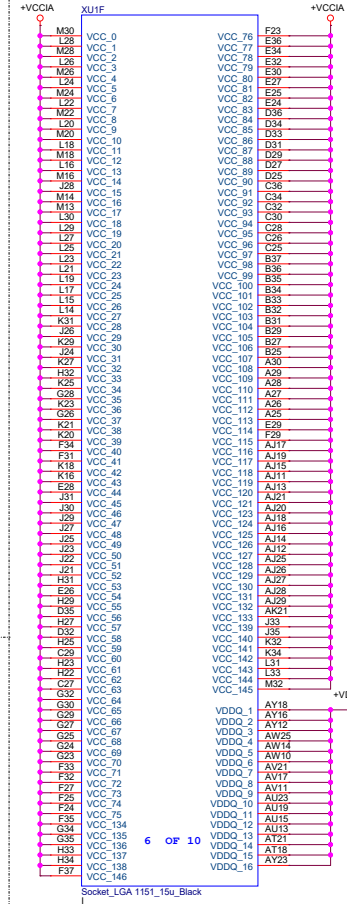
Design Note

VCCPLL, Iccmax=150mA / 1V
VCCST, Iccmax=80mA / 1V
VCCIO, Iccmax=6.4A / 0.95V
VCCGT, Iccmax=45A / 1.15V
VCCIA, Iccmax=79A / 1.15V
VDDQ, Iccmax=3.3A / 1.2V

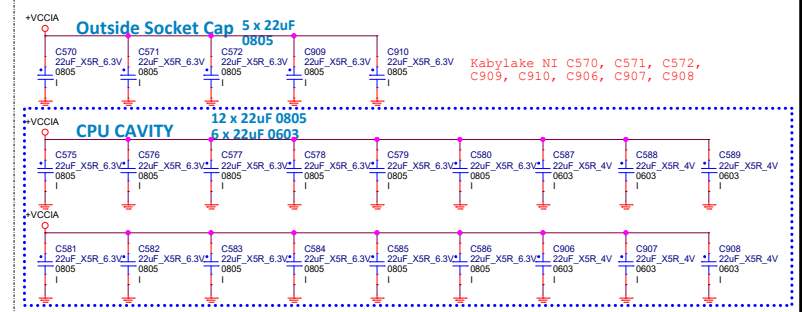
CPU - I part VCCGT and VCCSA



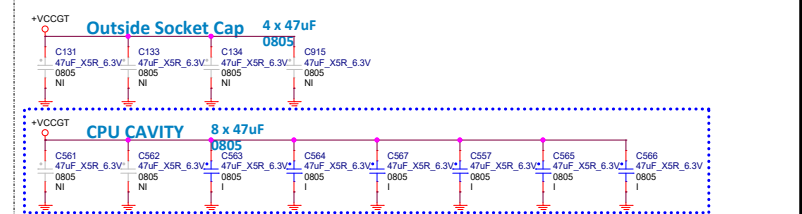
CPU - F part VCCIA



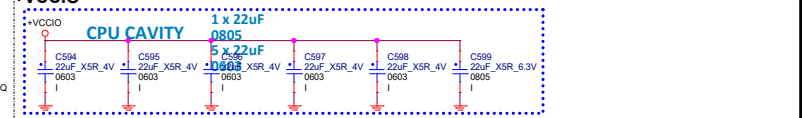
CPU CAPS VCCIA



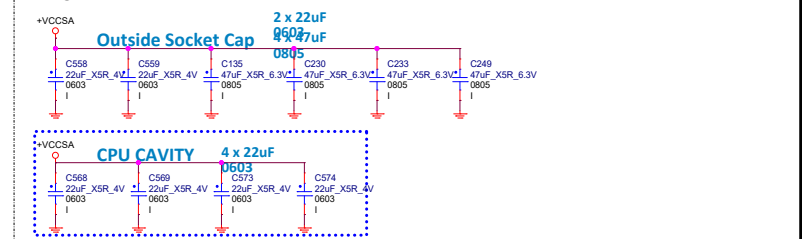
CPU CAPS +VCCGT



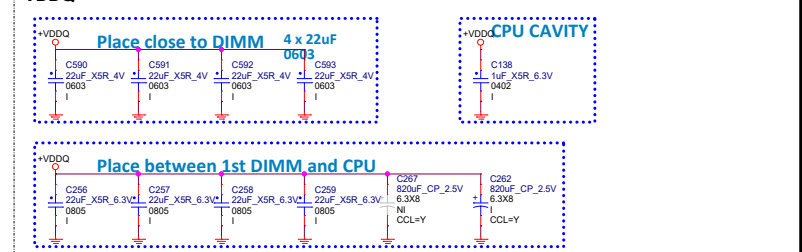
CPU CAPS +VCCIO



CPU CAPS +VCCSA



CPU CAPS +VDDQ



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Page Modified: Friday, July 05, 2019


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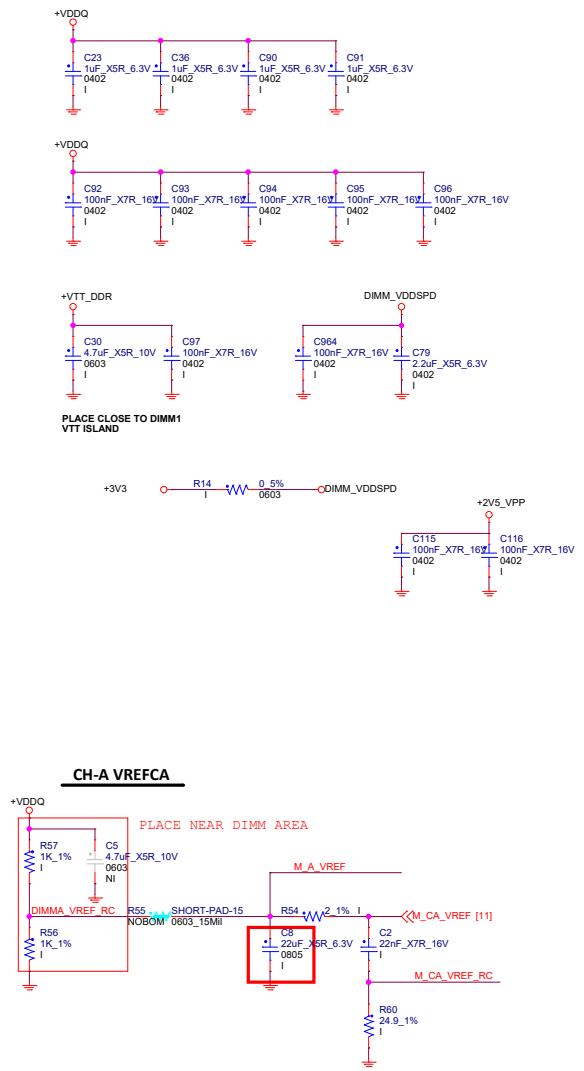
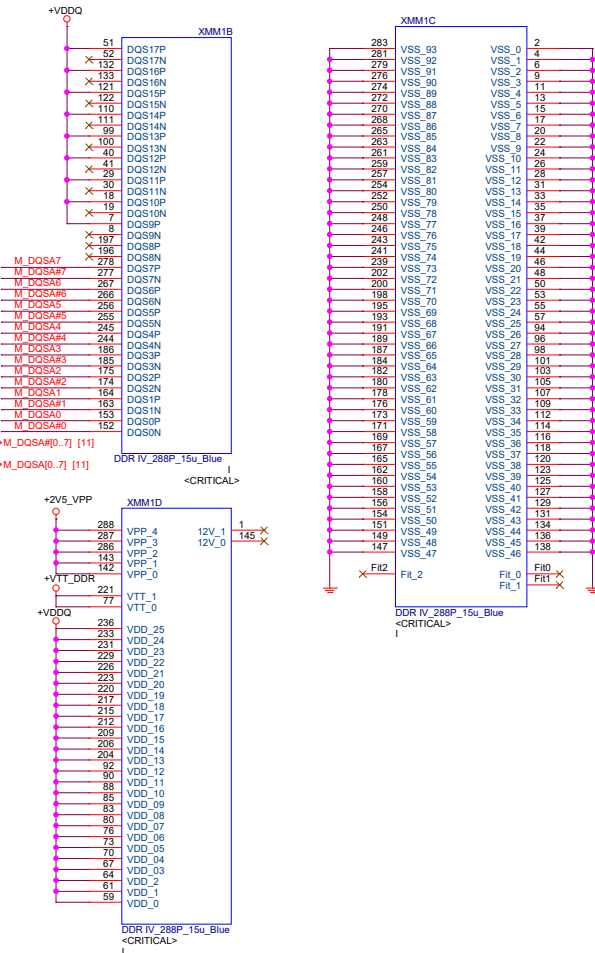
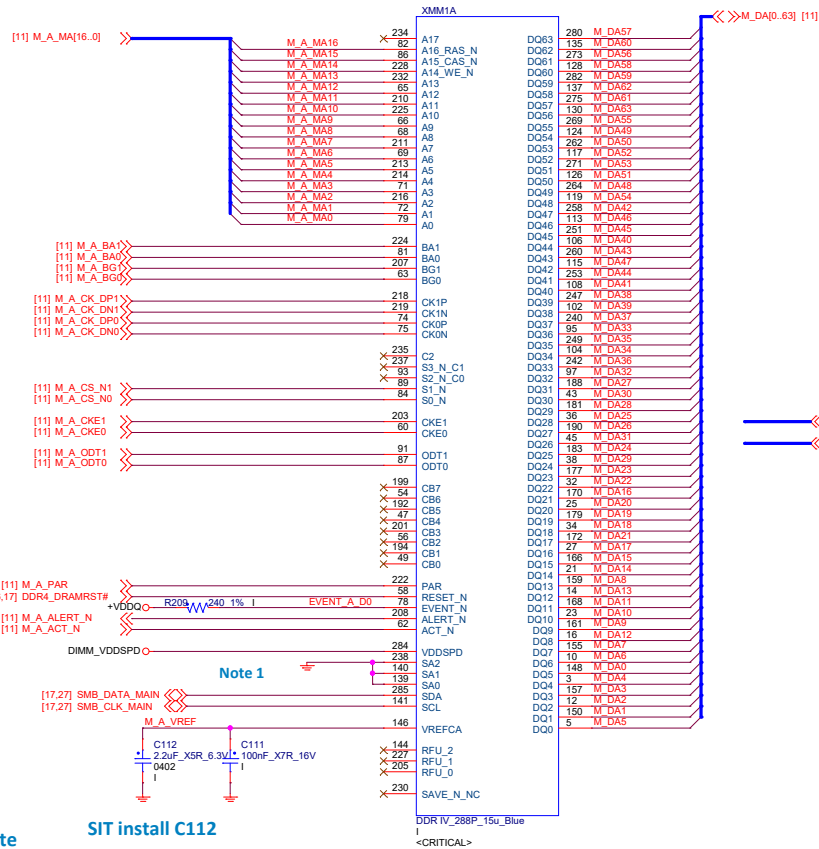
MCP- VSS

CPU - G/H part
VSS

XU1G										XU1H									
AW32	VSS_7	VSS_87	AN24	AW30	VSS_8	VSS_88	AN23	AW9	VSS_9	VSS_89	AN22	AH40	VSS_168	VSS_247	M4	AW5	VSS_10	VSS_90	AN19
AW3	VSS_11	VSS_91	AM17	AW34	VSS_12	VSS_92	AM16	AV30	VSS_13	VSS_93	AN11	AH38	VSS_169	VSS_248	L32	AV28	VSS_14	VSS_94	AH37
AV26	VSS_15	VSS_95	AN9	AV9	VSS_16	VSS_96	AN8	AV2	VSS_18	VSS_98	AN6	AG36	VSS_175	VSS_254	M17	AV3	VSS_19	VSS_99	AH36
AU34	VSS_20	VSS_100	AN5	AU30	VSS_21	VSS_101	AN4	AU7	VSS_22	VSS_102	AM40	AG33	VSS_176	VSS_255	M15	AU5	VSS_23	VSS_103	AH33
AU4	VSS_24	VSS_104	AM39	AU1	VSS_25	VSS_105	AF37	AT40	VSS_26	VSS_106	AM38	AG3	VSS_180	VSS_259	K30	AT39	VSS_27	VSS_107	AH32
AT39	VSS_28	VSS_108	AF36	AT38	VSS_29	VSS_109	AF35	AT36	VSS_30	VSS_110	AM37	AG5	VSS_181	VSS_260	L3	AT34	VSS_31	VSS_111	AM36
AT34	VSS_31	VSS_111	AF8	AT32	VSS_33	VSS_113	AF5	AT28	VSS_35	VSS_115	AM35	AG2	VSS_182	VSS_261	K28	AT27	VSS_36	VSS_116	AM34
AT27	VSS_37	VSS_117	AF1	AT26	VSS_38	VSS_118	AE36	AT24	VSS_39	VSS_119	AM34	AG1	VSS_183	VSS_262	K33	AT22	VSS_40	VSS_120	AM33
AT22	VSS_41	VSS_121	AE33	AT20	VSS_43	VSS_123	AE8	AT17	VSS_44	VSS_124	AM33	AG1	VSS_184	VSS_263	K33	AT14	VSS_45	VSS_125	AM32
AT14	VSS_46	VSS_126	AE5	AT12	VSS_47	VSS_127	AE3	AT10	VSS_48	VSS_128	AM32	AG1	VSS_185	VSS_264	K14	AT9	VSS_49	VSS_129	AM31
AT9	VSS_50	VSS_130	AD37	AT8	VSS_51	VSS_131	AD36	AT7	VSS_52	VSS_132	AM31	AG1	VSS_186	VSS_265	K7	AT6	VSS_53	VSS_133	AM30
AT6	VSS_54	VSS_134	AD35	AT5	VSS_55	VSS_135	AD34	AT4	VSS_56	VSS_136	AM30	AG1	VSS_187	VSS_266	K1	AT3	VSS_57	VSS_137	AM29
AR36	VSS_59	VSS_139	AD33	AR35	VSS_60	VSS_140	AD32	AR34	VSS_61	VSS_141	AM29	AG1	VSS_188	VSS_267	K26	AR33	VSS_62	VSS_142	AM28
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AR24	VSS_71	VSS_151	AD27	AR23	VSS_72	VSS_152	AD26	AR22	VSS_73	VSS_153	AM26	AG1	VSS_191	VSS_270	K22	AR21	VSS_74	VSS_154	AM25
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AW9	VSS_163	VSS_218	AD1	AW9	VSS_164	VSS_216	AD1	AW9	VSS_165	VSS_217	AM1	AG1	VSS_216	VSS_295	G13	AW9	VSS_157	VSS_203	AM0
AW9	VSS_166	VSS_219	AD1	AW9	VSS_167	VSS_217	AD1	AW9	VSS_168	VSS_218	AM0	AG1	VSS_217	VSS_296	G11	AW9	VSS_158	VSS_204	AM0
AW9	VSS_169	VSS_220	AD1	AW9	VSS_170	VSS_218	AD1	AW9	VSS_171	VSS_219	AM0	AG1	VSS_218	VSS_297	G6	AW9	VSS_159	VSS_205	AM0
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AW9	VSS_209	VSS_233	AD1	AW9	VSS_210	VSS_231	AD1	AW9	VSS_211	VSS_232	AM0	AG1	VSS_231	VSS_310	F1	AW9	VSS_172	VSS_218	AM0
AW9	VSS_212	VSS_234	AD1	AW9	VSS_213	VSS_232	AD1	AW9	VSS_214	VSS_233	AM0	AG1	VSS_232	VSS_311	D37	AW9	VSS_173	VSS_219	AM0
AW9	VSS_215	VSS_235	AD1	AW9	VSS_216	VSS_233	AD1	AW9	VSS_217	VSS_234	AM0	AG1	VSS_233	VSS_312	D30	AW9	VSS_174	VSS_220	AM0
AW9	VSS_218	VSS_236	AD1	AW9	VSS_219	VSS_234	AD1	AW9	VSS_220	VSS_235	AM0	AG1	VSS_234	VSS_313	E23	AW9	VSS_175	VSS_221	AM0
AW9	VSS_221	VSS_237	AD1	AW9	VSS_222	VSS_235	AD1	AW9	VSS_223	VSS_236	AM0	AG1	VSS_235	VSS_314	E21	AW9	VSS_176	VSS_222	AM0
AW9	VSS_224	VSS_238	AD1	AW9	VSS_225	VSS_236	AD1	AW9	VSS_226	VSS_237	AM0	AG1	VSS_236	VSS_315	E19	AW9	VSS_177	VSS_223	AM0
AW9	VSS_227	VSS_239	AD1	AW9	VSS_228	VSS_237	AD1	AW9	VSS_229	VSS_238	AM0	AG1	VSS_237	VSS_316	D28	AW9	VSS_178	VSS_224	AM0
AW9	VSS_230	VSS_240	AD1	AW9	VSS_231	VSS_238	AD1	AW9	VSS_232	VSS_239	AM0	AG1	VSS_238	VSS_317	E9	AW9	VSS_179	VSS_225	AM0
AW9	VSS_233	VSS_241	AD1	AW9	VSS_234	VSS_239	AD1	AW9	VSS_235	VSS_240	AM0	AG1	VSS_239	VSS_318	E6	AW9	VSS_180	VSS_226	AM0
AW9	VSS_236	VSS_242	AD1	AW9	VSS_237	VSS_240	AD1	AW9	VSS_238	VSS_241	AM0	AG1	VSS_240	VSS_319	E3	AW9	VSS_181	VSS_227	AM0
AW9	VSS_239	VSS_243	AD1	AW9	VSS_240	VSS_241	AD1	AW9	VSS_241	VSS_242	AM0	AG1	VSS_241	VSS_320	D39	AW9	VSS_182	VSS_228	AM0
AW9	VSS_242	VSS_244	AD1	AW9	VSS_243	VSS_242	AD1	AW9	VSS_242	VSS_243	AM0	AG1	VSS_242	VSS_321	D26	AW9	VSS_183	VSS_229	AM0
AW9	VSS_245	VSS_245	AD1	AW9	VSS_244	VSS_243	AD1	AW9	VSS_243	VSS_244	AM0	AG1	VSS_243	VSS_322	D24	AW9	VSS_184	VSS_230	AM0
AW9	VSS_248	VSS_246	AD1	AW9	VSS_245	VSS_244													

1	2	3	4	5	6	7	8
A							A
B							B
C							C
D							D
1	2	3	4	5	6	7	8

		Hon Hai Precision Industry Co. Ltd.	
Foxconn NPCEBG		Phone: 027-59603888	
Foxconn WuHan		Fax:	
China			
Title			
15. BLANK			
Size	Document Number		Rev
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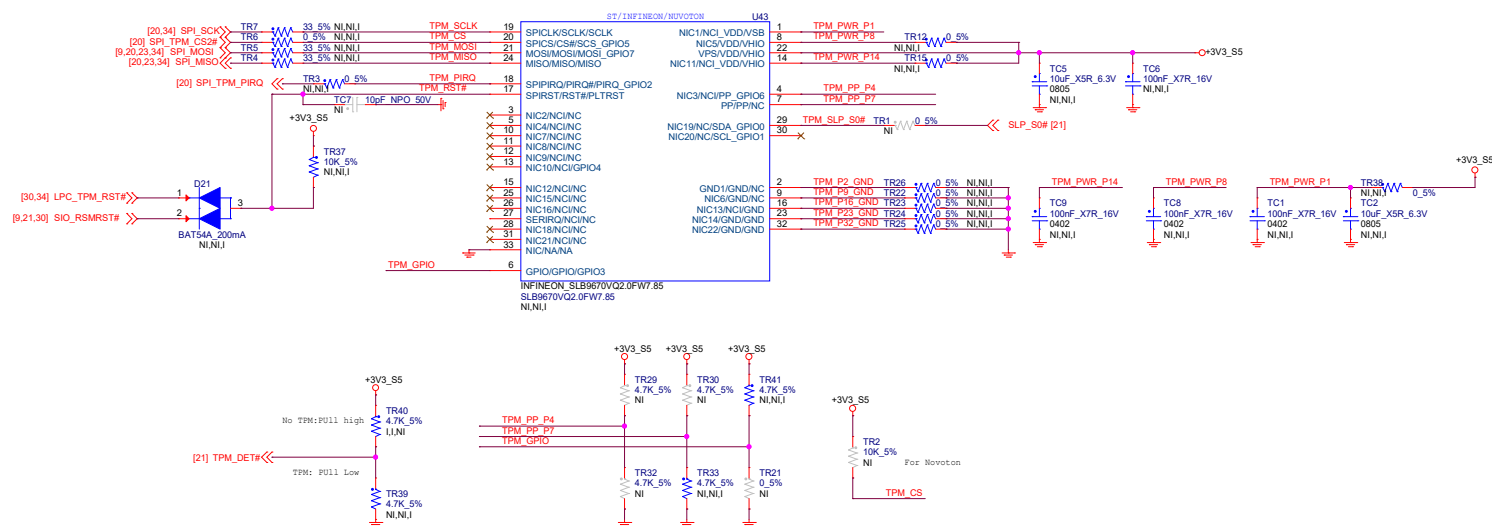




TPM-SPI Interface

TPM
ST & NCT & Infineon co-lay
NPCT750LBAYX
ST33HTPH2E32AHB4
SLB9670VQ2.0FW7.62

PIN	SLB9670VQ2.0FW7.62	NPCT750	ST33HTPH2E32AHB4
1	TR38/TC1/TC2	TR38/TC1/TC2	NI
2	TR26	NI	TR26
7	TR33	NI	NI
8	TR12/TC8	TR12/TC8	NI
9	TR22	TR22	NI
14	TR15/TC9	TR15/TC9	NI
16	TR23	TR23	NI
23	TR24	TR24	NI
27	NI	TR39	NI
29	NI	TR1	NI
32	TR25	TR25	NI

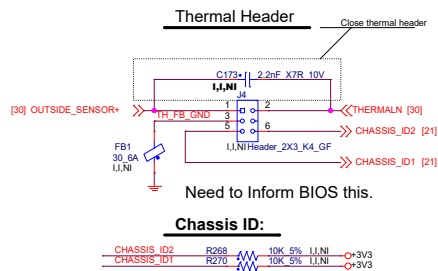
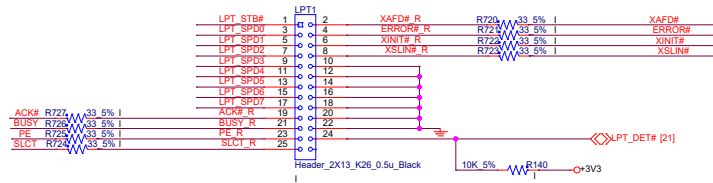
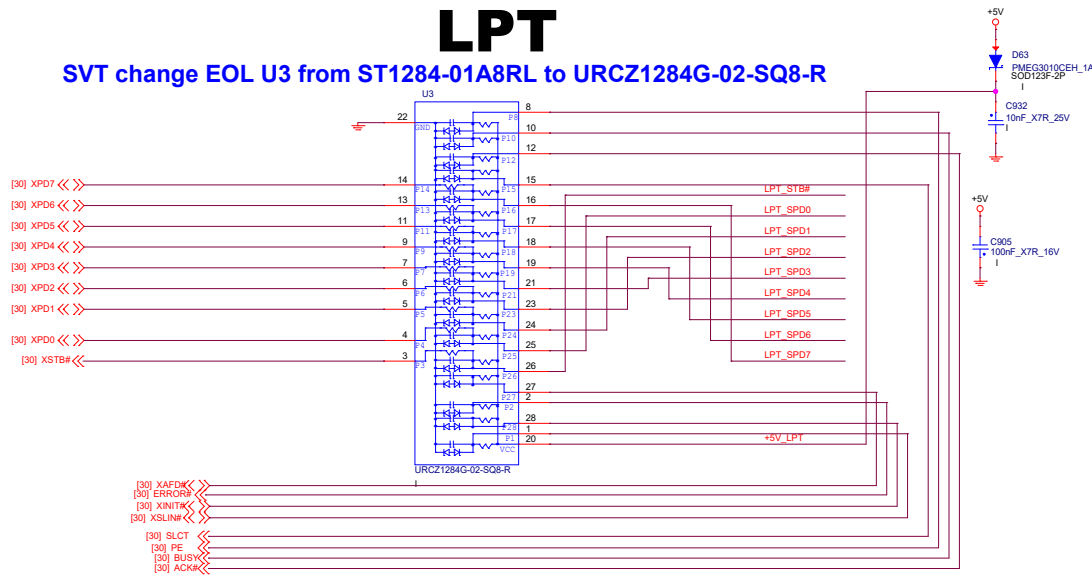


BOM DISTRIBUTION RULE

QT,SMB&Consumer,Think M70e
(BOM, BOM, BOM)

LPT

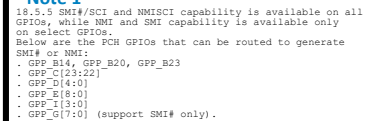
SVT change EOL U3 from ST1284-01A8RL to URCZ1284G-02-SQ8-R



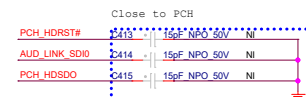
	Chassis ID1	Chassis ID2
25L	1 (Empty)	1 (Empty)
17L	1 (Empty)	0 (GND)
20L (New)	0	1
13L	0	0
10L	0	0

Waiting Update

Design Note



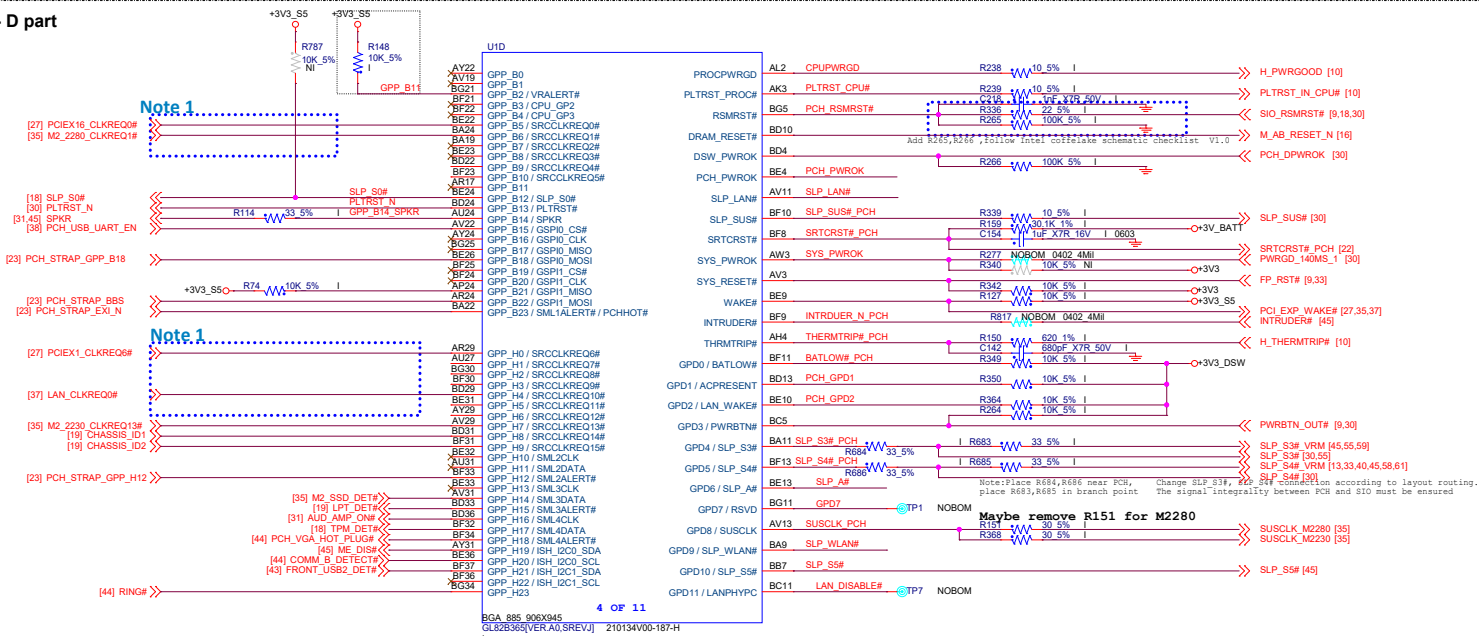
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		Hon Hai Precision Industry Co. Ltd.	
Foxconn NPCEBG Foxconn Wuhan China		Phone: 027-59603888 Fax:	
Title			
20. PCH - LPC/HDA/SMB/GPIO			
Size C	Document Number B365_SFF		Rev SVT
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PCH - GPIO/SEQUENCE

PCH - D part



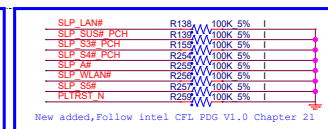
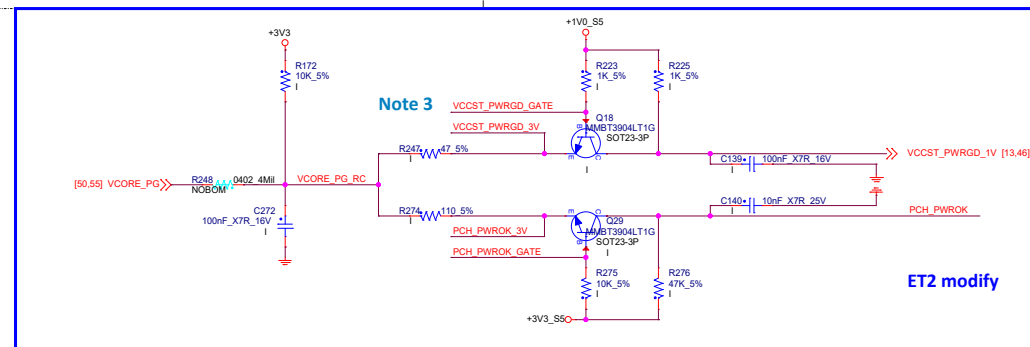
Design Note

Note 1

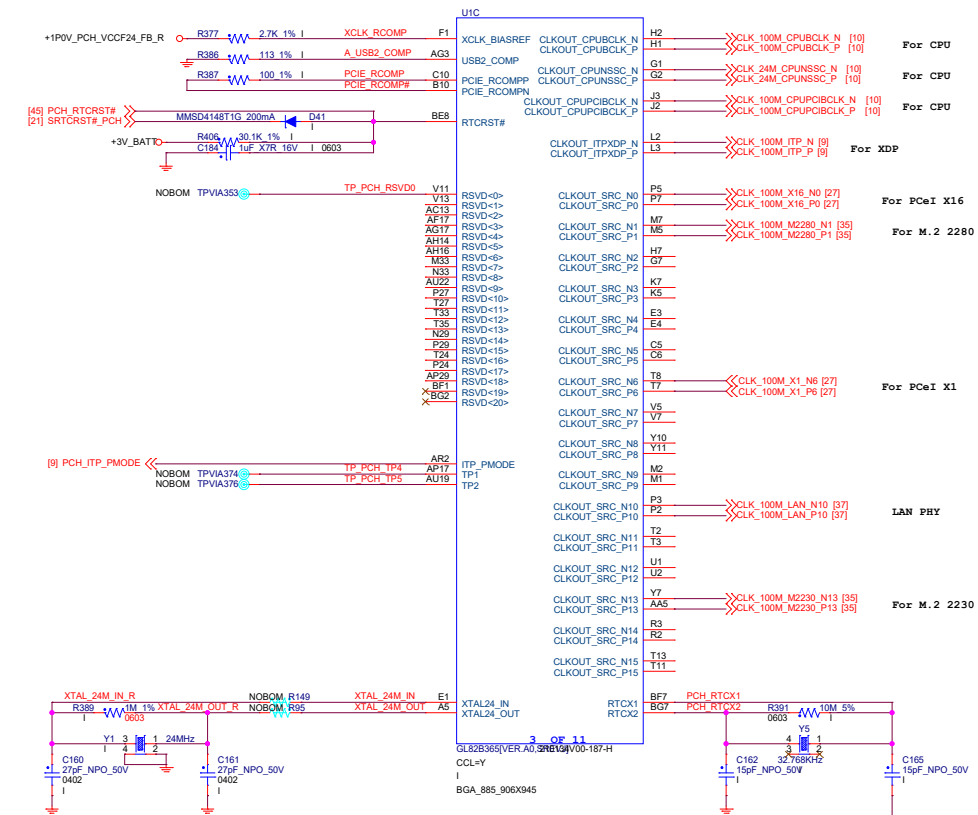
SRCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements

SRCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs

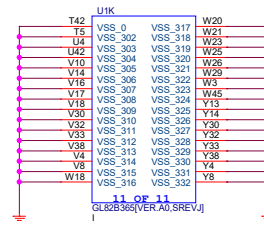
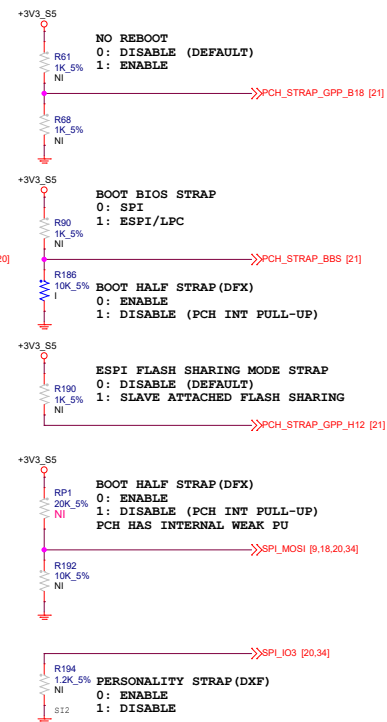
SRCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs



PCH - CLOCK

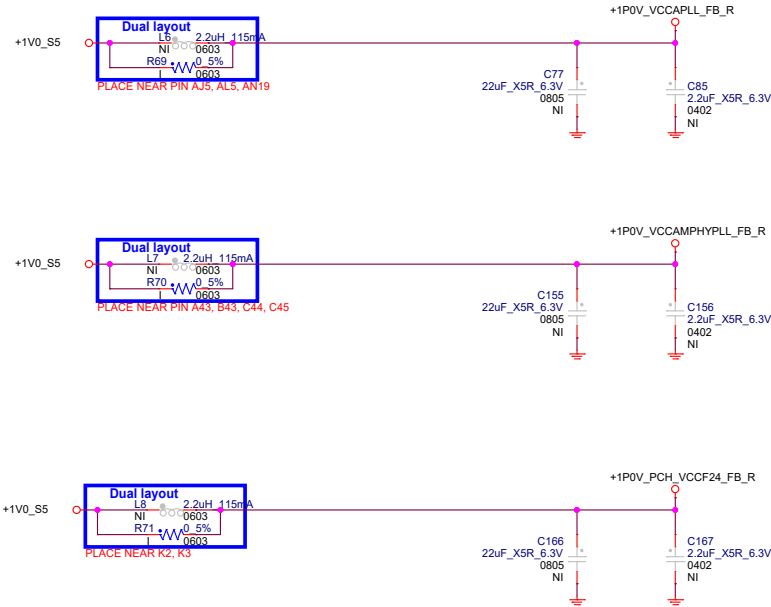


SIT change C160, C161 from 22pF to 27pF

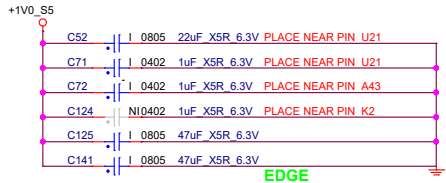


SKYLAKE Decoupling & filter

FILTER



V1.0A



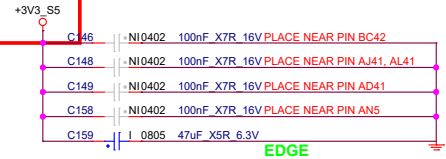
V3.3 DSW



VccPGPPA



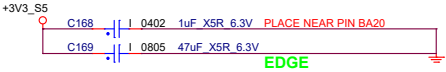
V3.3A



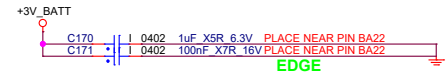
V1.8A / V1.8S / V3.3S



V3.3A



VCCRTC

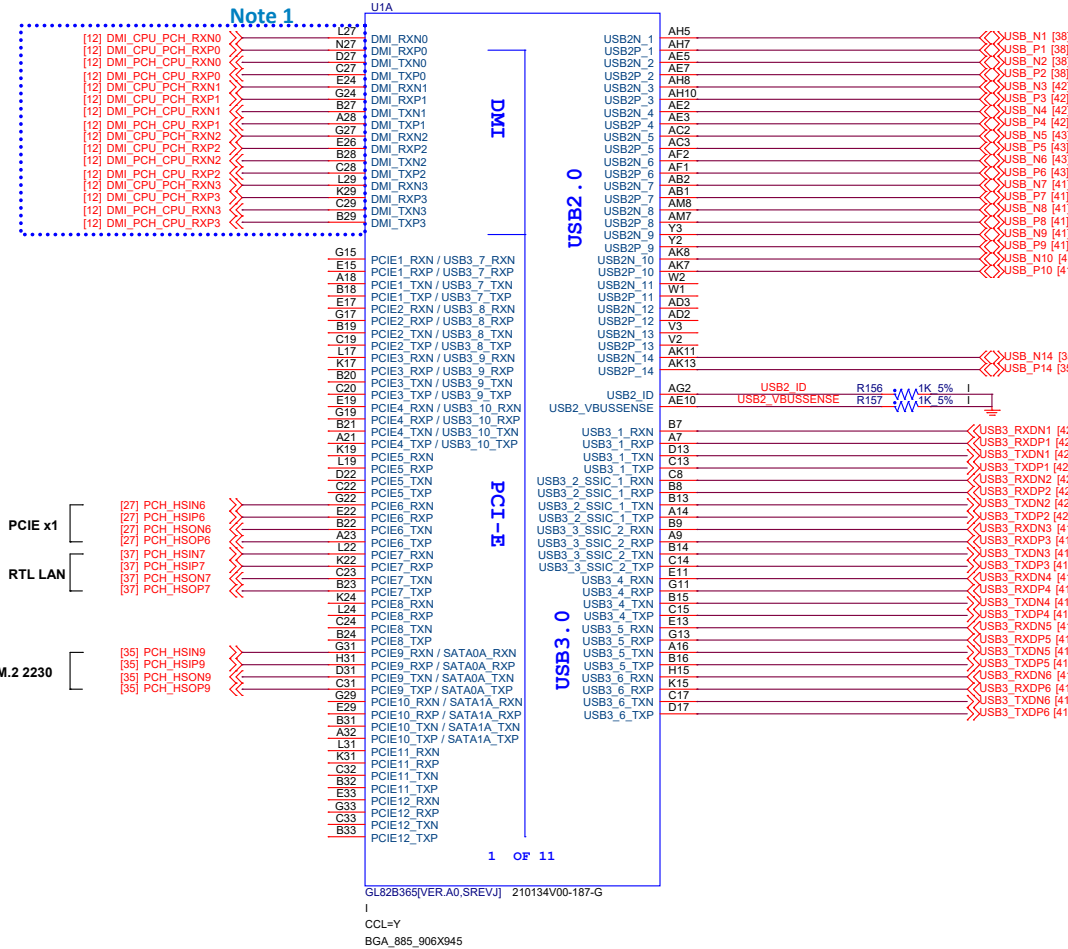


Power Plane Isolation

Need to update for KBL

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16
		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
PCH 3.3V Standby	AZALIA	AW26
	USB3	P20
	RTC	AP35
	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
PCH 3.3V	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

PCH - DMI/PCIE/USB2-3



Design Note

Note 1

According to Intel's update
DMI@PCH can not have lane reversal

- LAN+USB2
- LAN+USB2
- Rear USB3.0
- Rear USB3.0
- Card Reader Header
- Card Reader Header
- FRONT IO USB3.1 G1
- FRONT IO USB3
- FRONT IO USB3.1 G1
- FRONT IO USB3

M2 2230

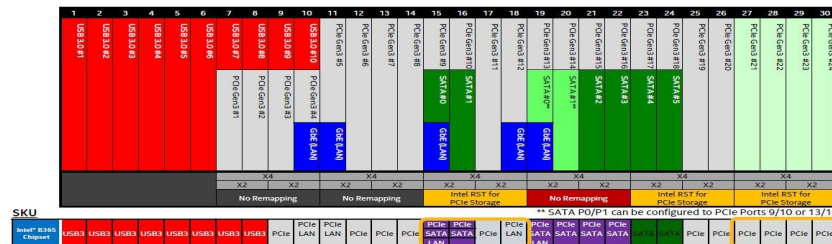
- Rear USB3.0
- Rear USB3.0
- FRONT IO USB3.1 G1
- FRONT IO USB3.1 G1
- FRONT IO USB3
- FRONT IO USB3

B365 USB3.0

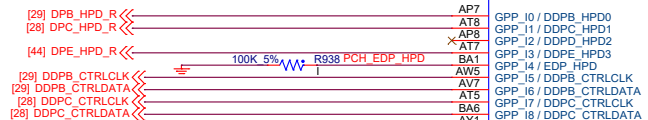
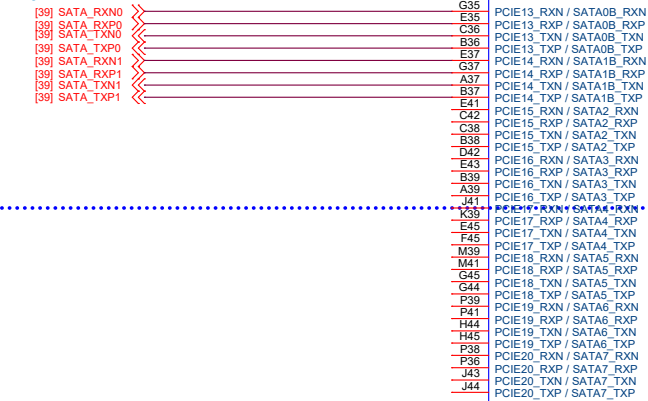
B365 USB3.1 G1

B365 USB3.0

Intel® B365 Chipset HSIO Lane Assignments



PCH - SATA/PCIE/HPD/GPIO



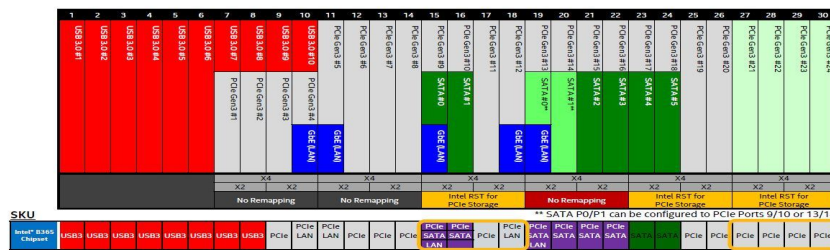
M.2 2280

2 OF 11

GL82B365[VER.A0,SREVJ] 210134V00-187-H

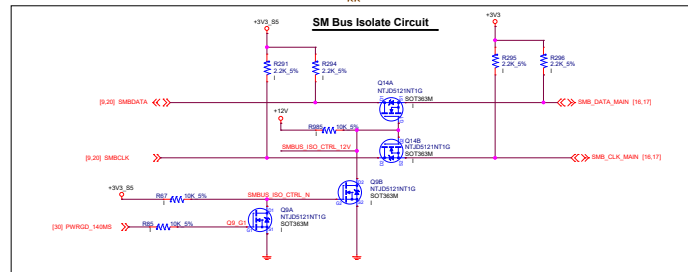
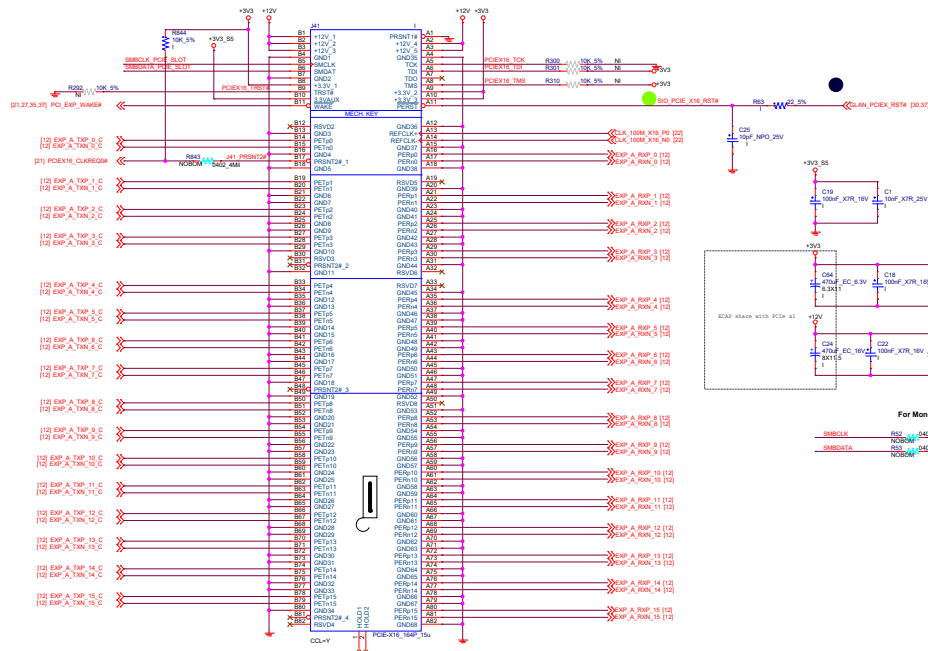
CCL=Y
BGA 885 906X945

Intel® B365 Chipset HSIO Lane Assignments

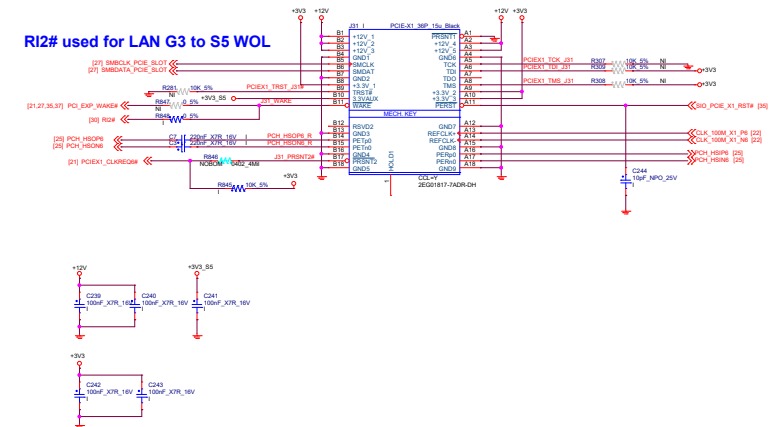


 Foxconn® Foxconn NPCEBG Foxconn Wuhan China		Hon Hai Precision Industry Co. Ltd. Phone: 027-59603888 Fax:	
Title 26. PCH - SATA/PCIE/GPIO			
Size	Custom	Document Number	Rev
		B365_SFF	SVT
Page Modified: Friday, July 05, 2019		17:16:33 (UTC+08C)	Sheet 26 of 65

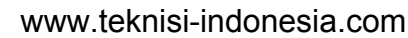
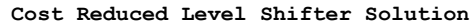
PCI EXPRESS x16 SLOT

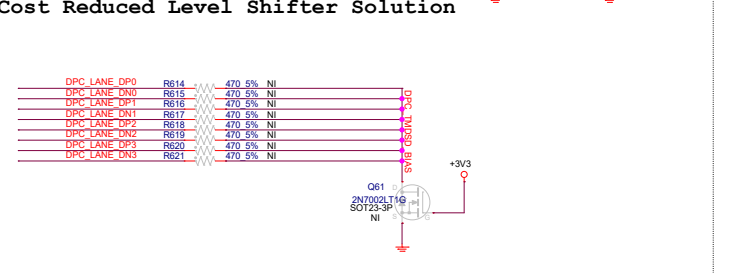
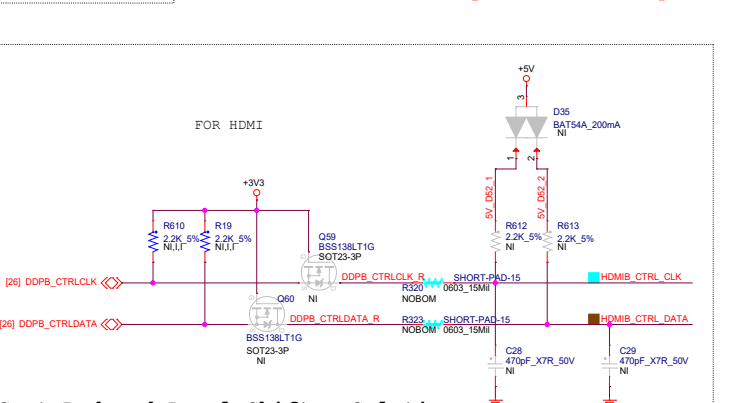
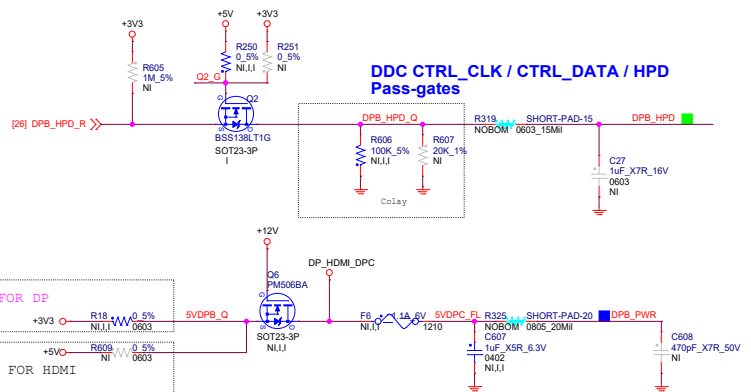
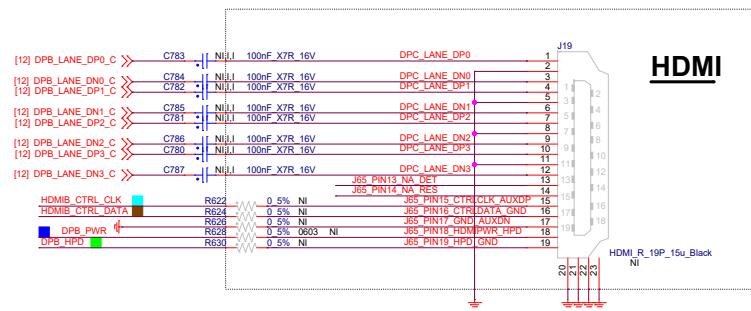


PCI EXPRESS X1 SLOT1(Support Gen3)

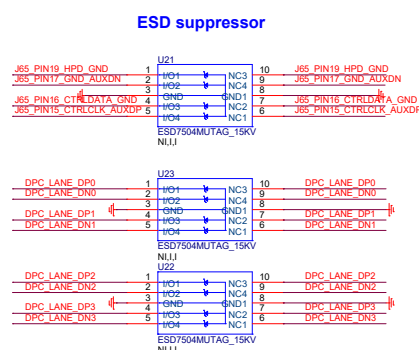
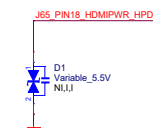


C772 100F X7R 16V LLNI TMDS02 DATA2# 1 D2+
 C773 100F X7R 16V LLNI TMDS03 DATA2# 2 GND_P2
 C776 100F X7R 16V LLNI TMDS04 DATA1# 3 D2-
 C768 100F X7R 16V LLNI TMDS05 DATA1# 4 D1+
 C765 100F X7R 16V LLNI TMDS06 DATA0# 5 GND_P5
 C774 100F X7R 16V LLNI TMDS07 DATA0# 6 D1-
 C771 100F X7R 16V LLNI TMDS08 DATA0# 7 GND_P8
 C770 100F X7R 16V LLNI TMDS09 CLK# 8 D2+
 HDMIC_CTRL_CLK 9 OK
 HDMIC_CTRL_DATA 10 GND_P11
 DPC_PWR 11 CEC
 DPC_HPD 12 RSVD
 13 SCL
 14 SDA
 15 -V
 16 GND_P17
 17 B_GND3
 18 B_GND3
 19 B_GND3
 20 NPTH
 21 NPTH
 22 NPTH
 23 NPTH
 24 NPTH
 25 NPTH
 26 NPTH
 27 NPTH
 28 NPTH

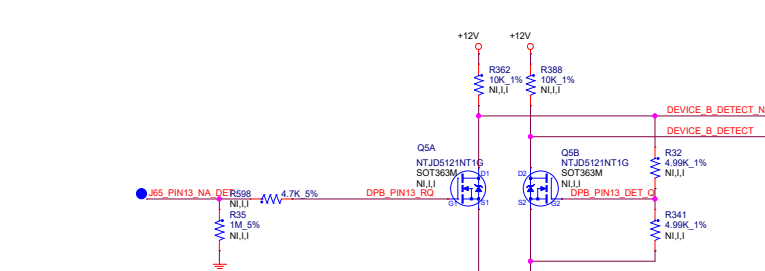
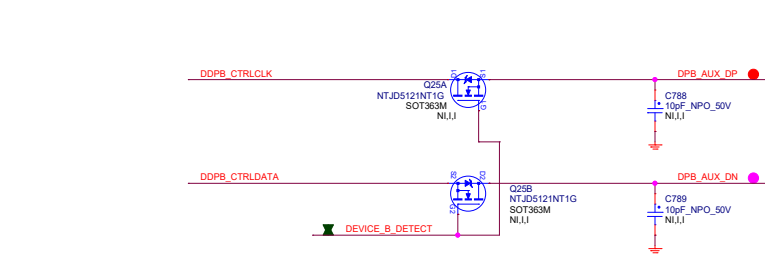
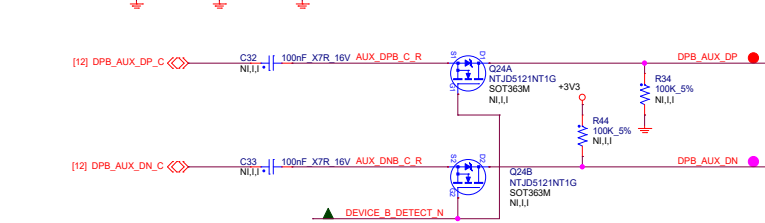
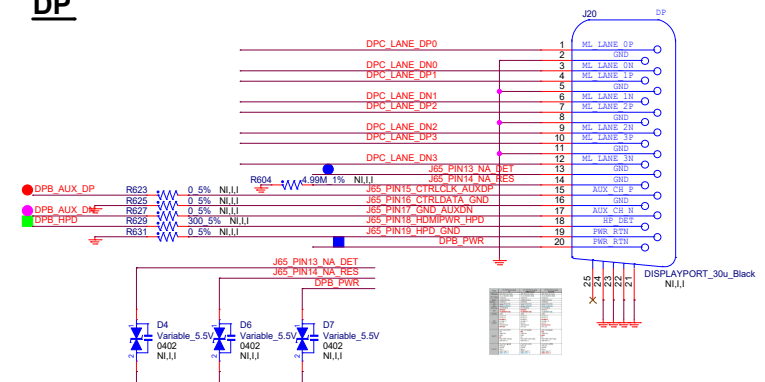




HDMI : Green
DP : Pink



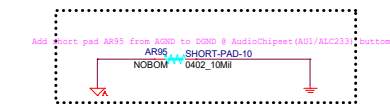
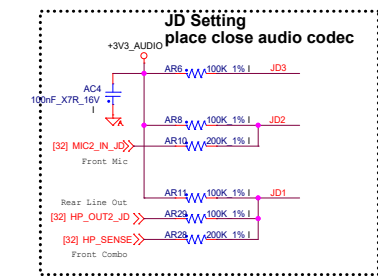
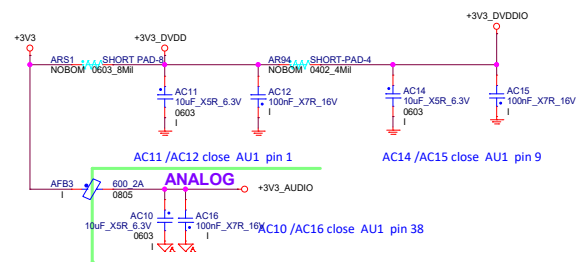
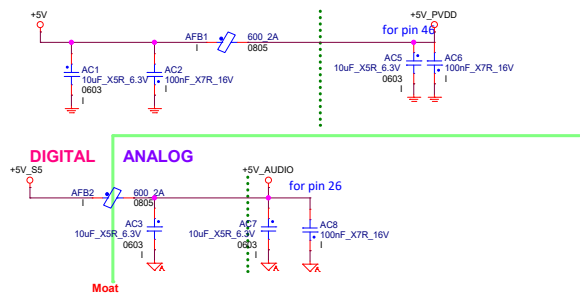
DP



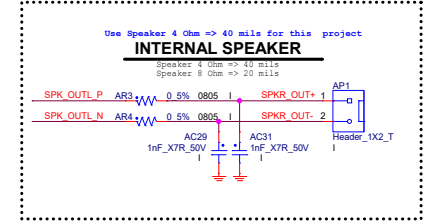
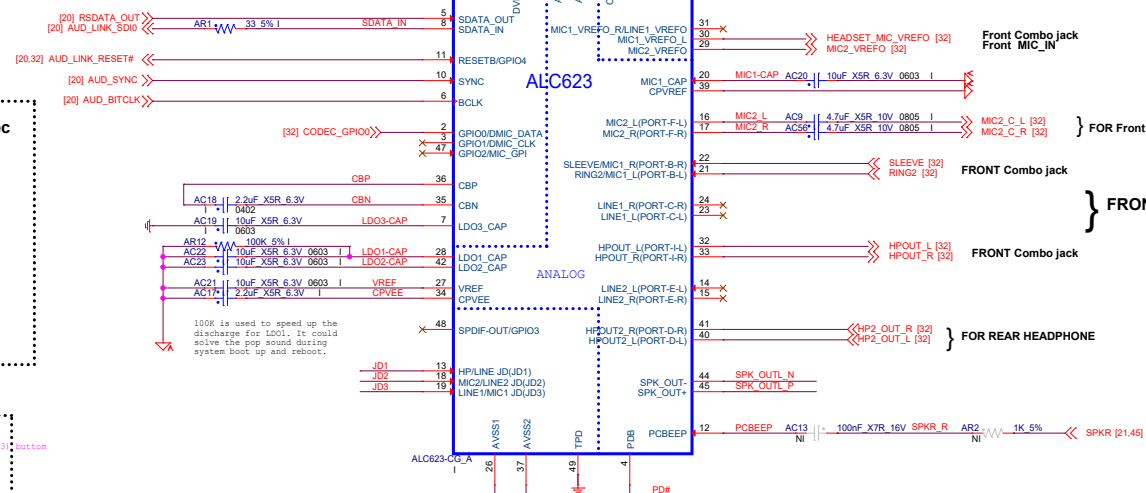
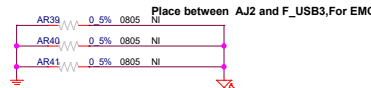
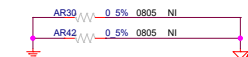
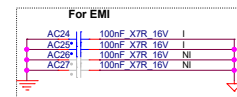
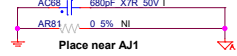
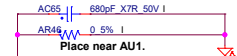
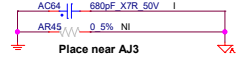
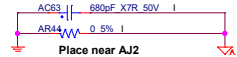
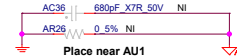
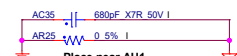
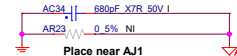
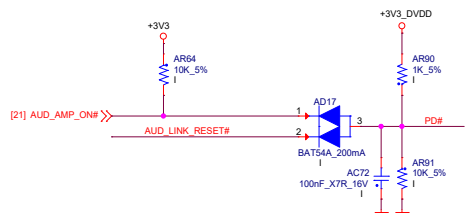
PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 68h default value always 80h)



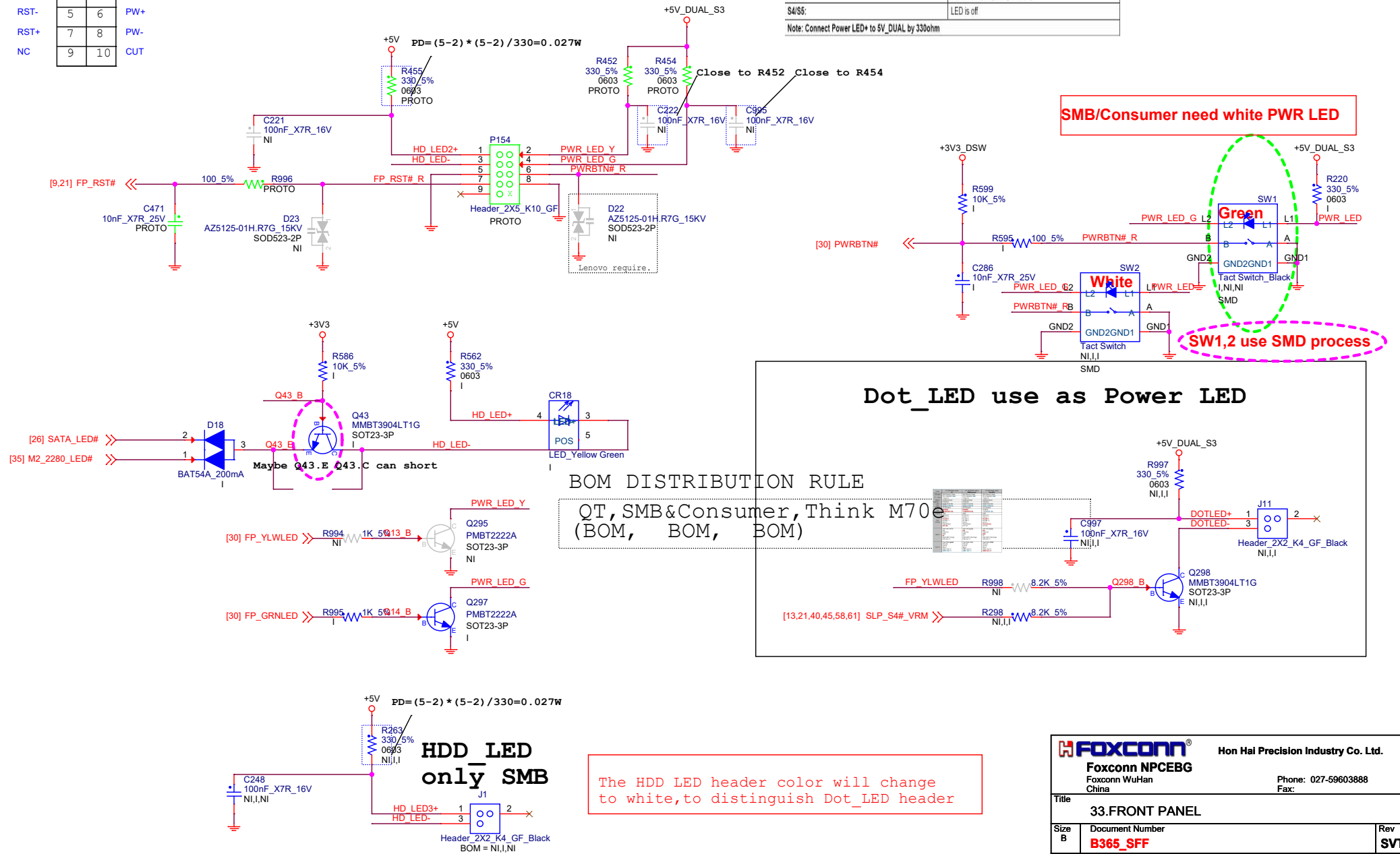


AMP ENABLE CIRCUIT



2-Pin single color LED	
S0:	LED is on steady green
S1/S3:	LED blinks(frequency: 1Hz/S)
S4/S5:	LED is off


Note: Connect Power LED+ to 5V_DUAL by 330ohm



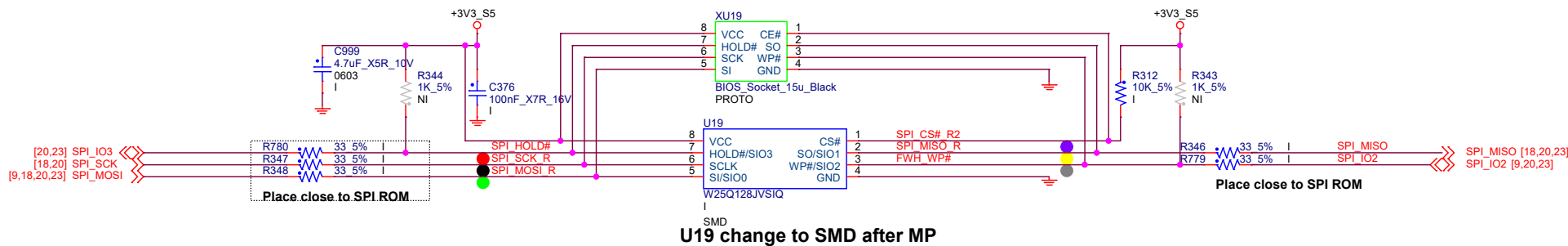
BOM DISTRIBUTION RULE

QT, SMB&Consumer, Think M70e
(BOM, BOM, BOM)

Dot LED use as Power LED

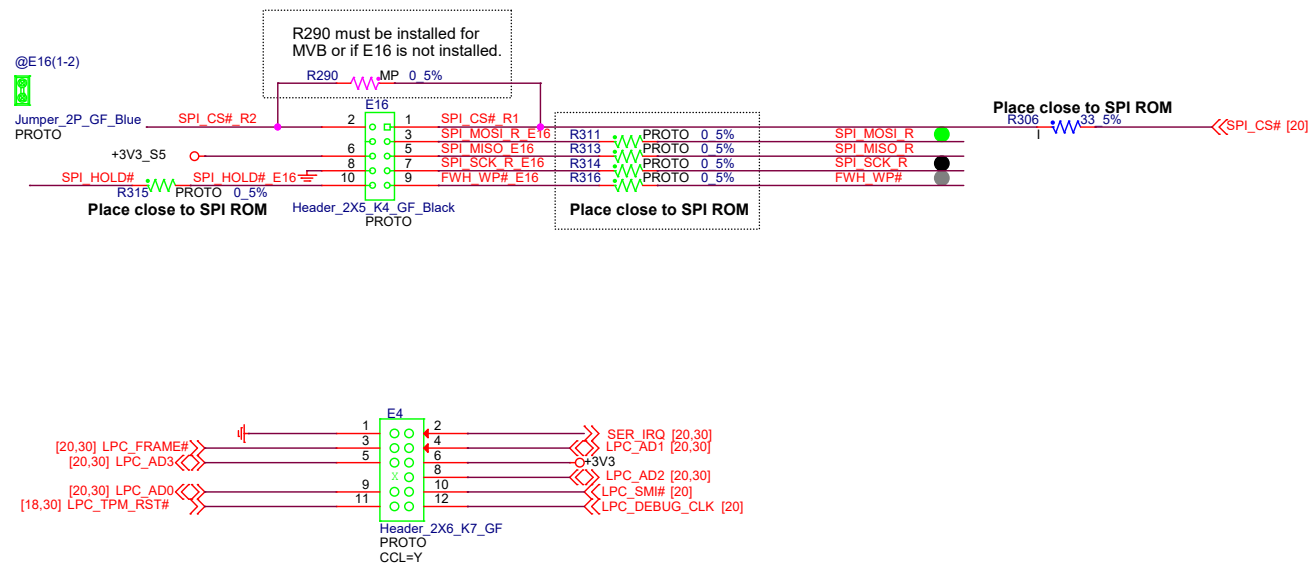
		Hon Hai Precision Industry Co. Ltd.	
Foxconn NPCEBG Foxconn WuHan China		Phone: 027-59603888 Fax:	
Title 33.FRONT PANEL			
Size B	Document Number B365_SFF		Rev SV
Page Modified: Friday, July 05, 2019		17:32:56 (UTC/GMT)	Sheet 33 of 65


SPI ROM



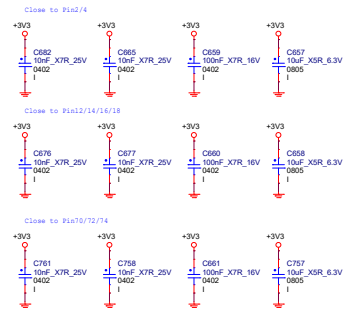
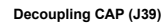
FOXCONN SPI ROM DEBUG HEADER

The header traces should be daisy-chain through the header with no stubs.



 FOXCONN®		Hon Hai Precision Industry Co. Ltd.	
Foxconn NPCEBG			
Foxconn WuHan		Phone: 027-59603888	
China		Fax:	
Title			
34.SPI ROM & SPI DEBUG*			
Size B	Document Number B365_SFF		Rev SVT
Page Modified: Friday, July 05, 2019		17:24:29 (UTC/GMT)	Sheet 34 of 65

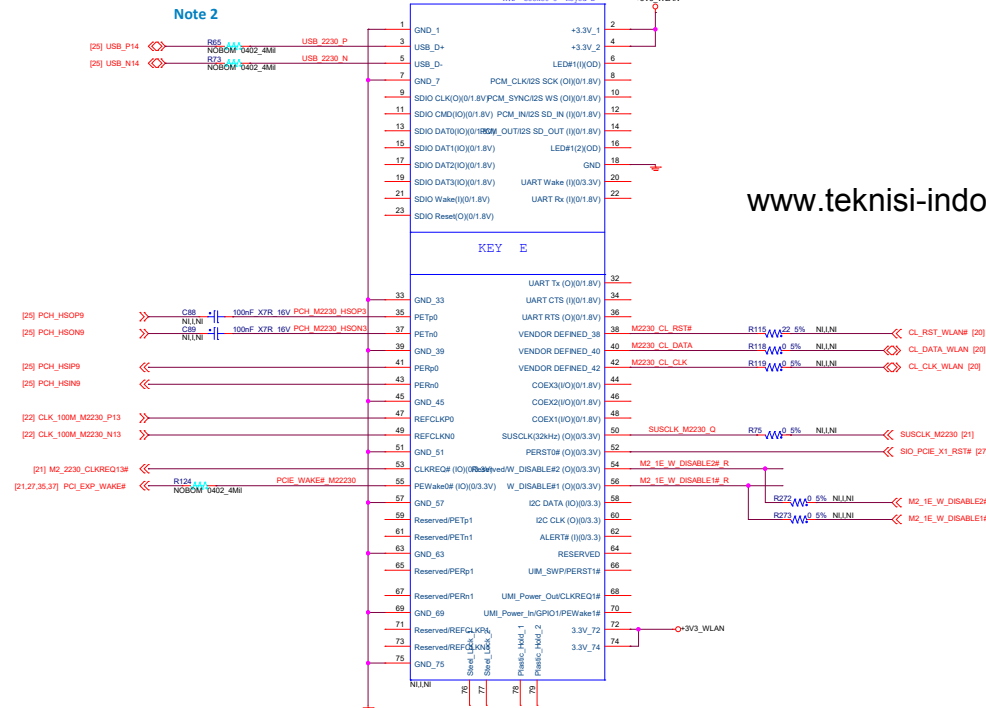
white color



M.2 SSD PU/PD Config

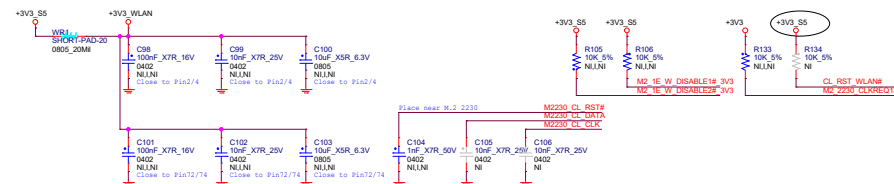


LED Res	Power Rating(W)
Spec	0.0625
Actual	0.0075



```
QT,SMB&Consumer,Think M70e
(BOM,  BOM,  BOM)
```

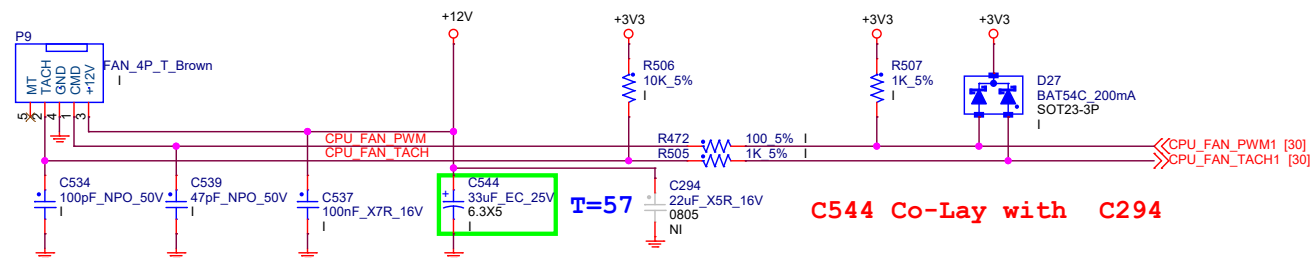
M.2 HW Config and Power Cap



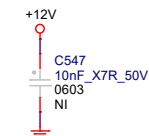
 FOXCONN® Foxconn NPCEBG Foxconn Wuhan China		Hon Hai Precision Industry Co. Ltd. Phone: 027-59603888 Fax:	
Title <div style="border: 1px solid black; padding: 5px; text-align: center;"> 35. M2.2280 & M.2 2230 </div>			
Size	Document Number		Rev
Cust	B365 SFF		05
Page Modified: Friday, July 05, 2019		7 10:30 (UTC+8GMT)	Sheet 35 of 65

CPU FAN

Color: Brown
Follow DTDL

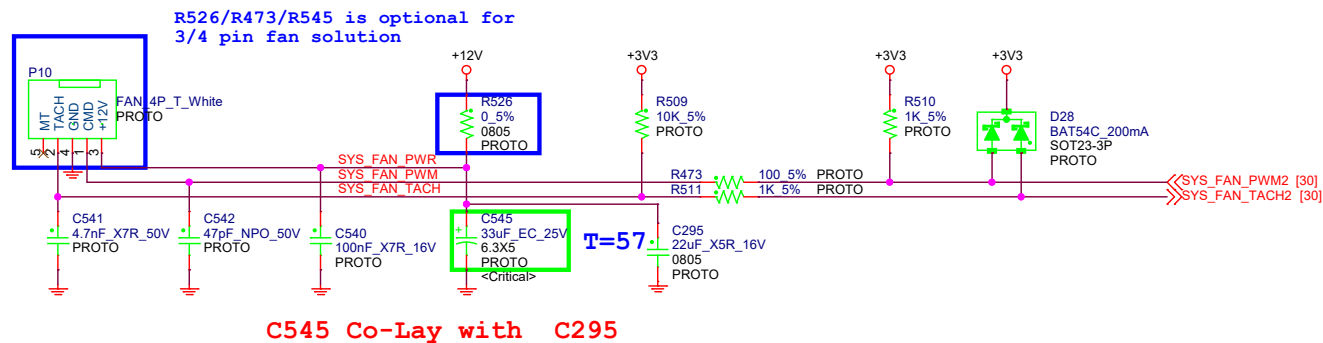



For EMI

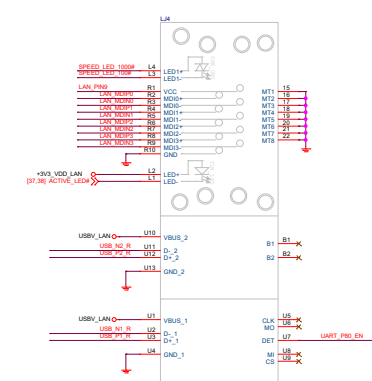
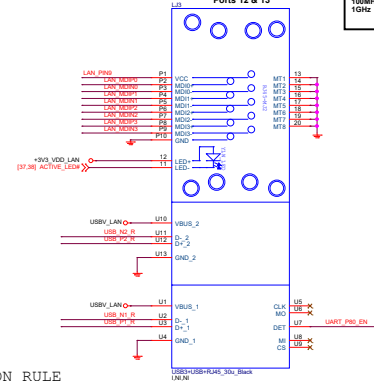


SYSTEM FAN

Color: White
Follow DTDL

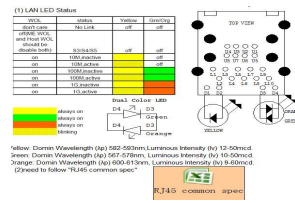


 FOXCONN® Foxconn NPCEBG Foxconn WuHan China		Hon Hai Precision Industry Co. Ltd. Phone: 027-59603888 Fax:	
Title 36.FAN HEADERS			
Size B	Document Number B365_SFF		Rev SVT
Page Modified: Friday, July 05, 2019		17:10:33 (UTC/GMT)	Sheet 36 of 65



Surge for LC

Non surge for LI (UDE source)



12 definition for LG

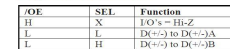
(1) LANI LED Status

(2) Yellow: Domin Wavelength (lp) 582-593nm, Luminous Intensity (lv) 12-50mcd

WOL	status	Yellow
don't care	No Link	off
offline WOL and Host WOL should be (disable both)	S3/S4/S5	off
on	10M inactive	
on	10M active	
on	100M inactive	
on	100M active	
on	1G inactive	
on	1G active	

always on

blinking



LAN MDIO 10
LAN MDIO 9
LAN MDIO 8
LAN MDIO 7
LAN MDIO 6

NC3
NC4
GND
NC2
NC1

1
2
3
4
5

LAN MDIO 1
LAN MDIO 2
LAN MDIO 3
LAN MDIO 4
LAN MDIO 5

EBD7504MUTAG_15KV

NI

LAN MDIO 10
LAN MDIO 9
LAN MDIO 8
LAN MDIO 7
LAN MDIO 6

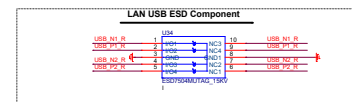
NC3
NC4
GND
NC2
NC1

1
2
3
4
5

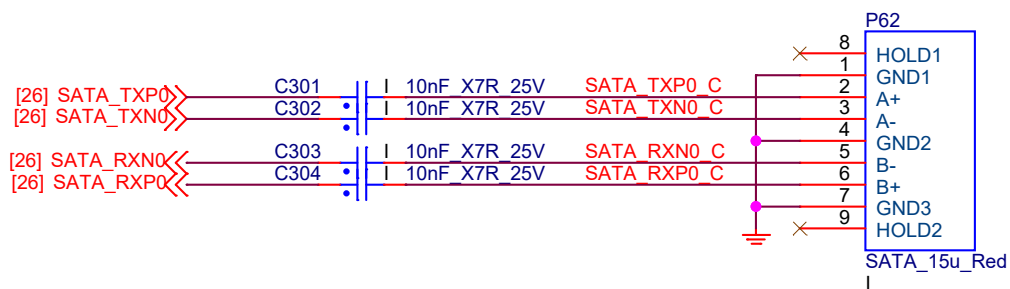
LAN MDIO 1
LAN MDIO 2
LAN MDIO 3
LAN MDIO 4
LAN MDIO 5

EBD7504MUTAG_15KV

NI



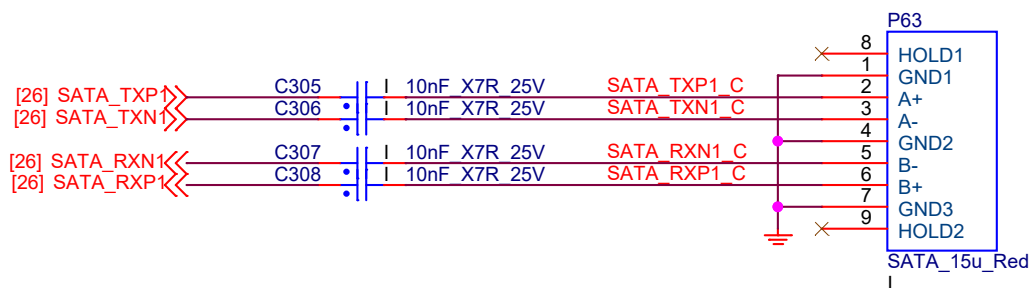
SATA 3.0 Port0,1



SATA GEN3.0



RED



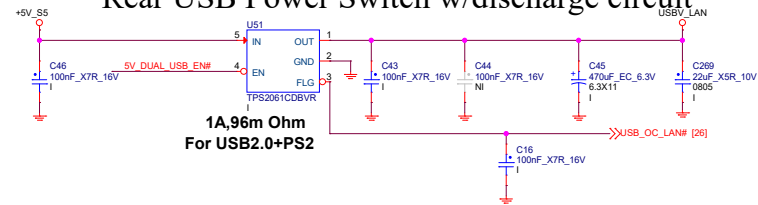
SATA GEN3.0



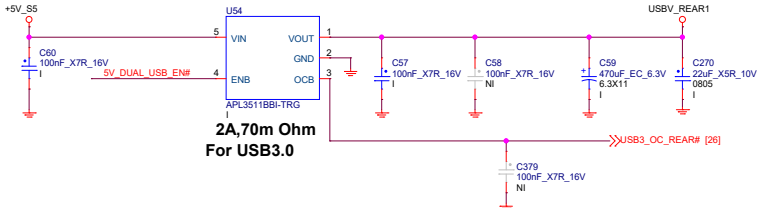
RED

 Foxconn NPCEBG Foxconn WuHan China		Hon Hai Precision Industry Co. Ltd. Phone: 027-59603888 Fax:	
Title			
39.SATA			
Size A	Document Number B365_SFF		Rev SVT
Page Modified: Friday, July 05, 2019		17:10:33 (UTC/GMT)	Sheet 39 of 65

Rear USB Power Switch w/discharge circuit

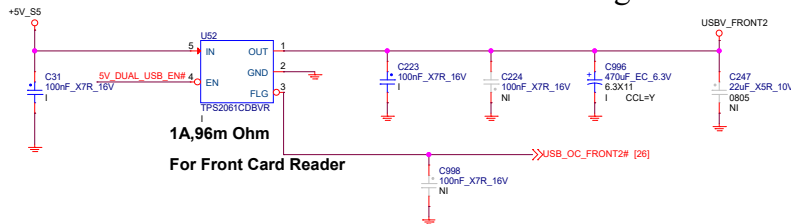


1A,96m Ohm
For USB2.0+PS2



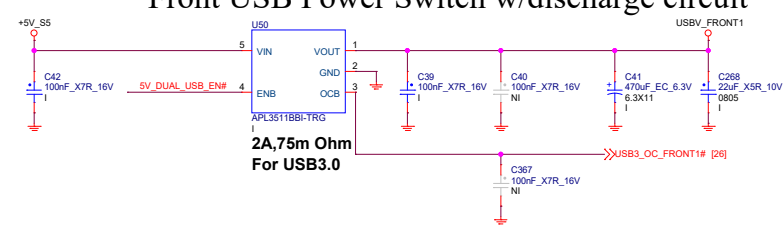
2A,70m Ohm
For USB3.0

Internal USB Power Switch w/discharge circuit



1A,96m Ohm
For Front Card Reader

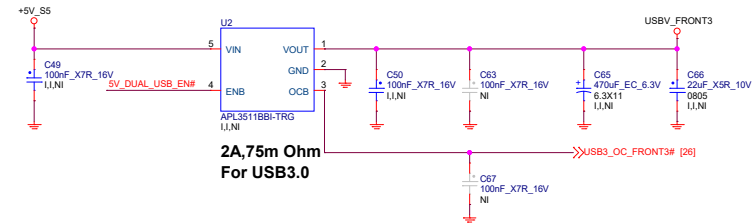
Front USB Power Switch w/discharge circuit



2A,75m Ohm
For USB3.0

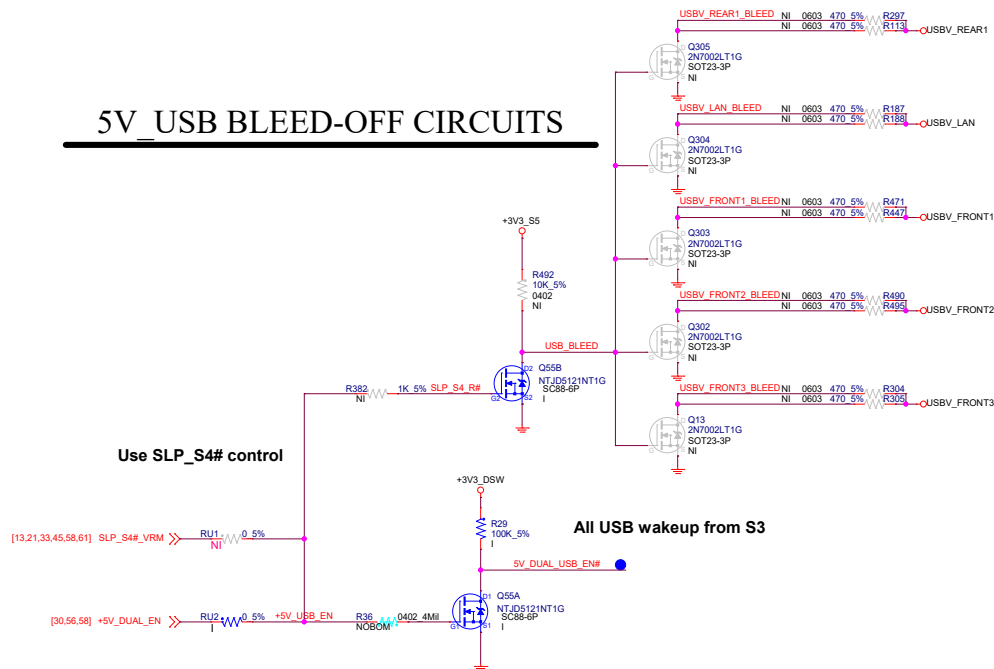
BOM DISTRIBUTION RULE

QT,SMB&Consumer,Think M70e
(BOM, BOM, BOM)



2A,75m Ohm
For USB3.0

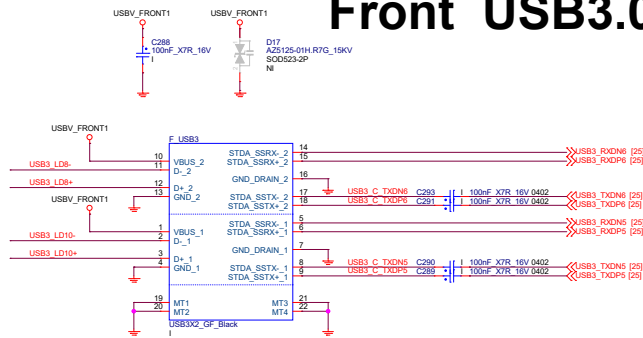
5V_USB BLEED-OFF CIRCUITS



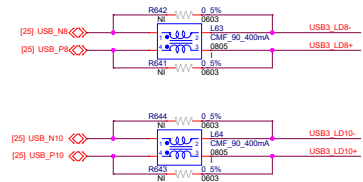
Use SLP_S4# control

All USB wakeup from S3

Front USB3.0X2

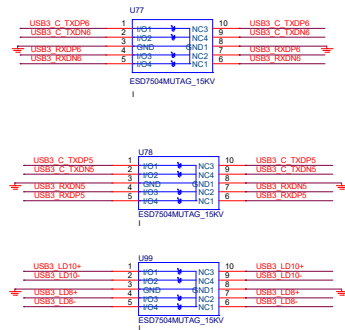


BLACK



Remove the CMC/0ohm co-layer solution for USB3 signals in SIT phase

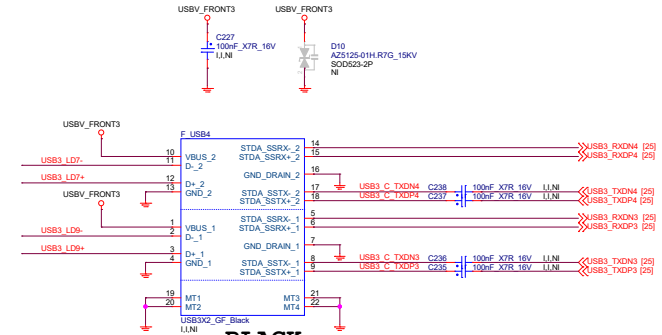
ESD suppressor



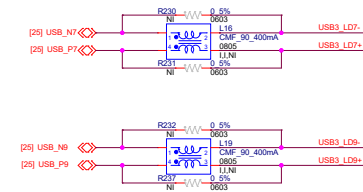
Front USB3.1 gen1

BOM DISTRIBUTION RULE

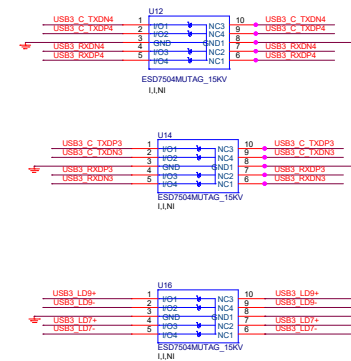
QT, SMB&Consumer, Think M70e
(BOM, BOM, BOM)



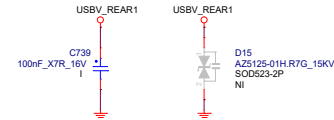
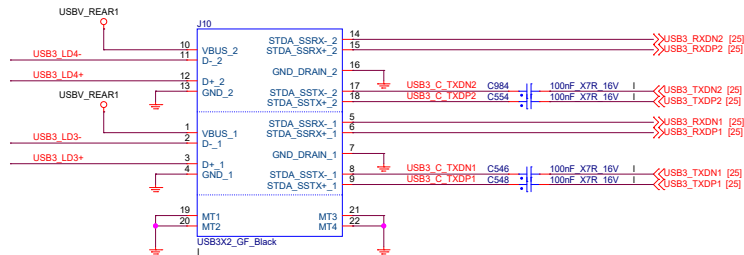
BLACK
BLUE



ESD suppressor

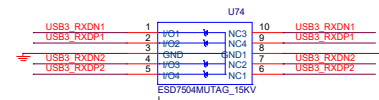
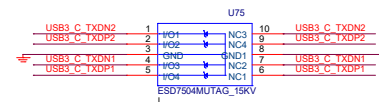
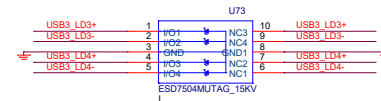
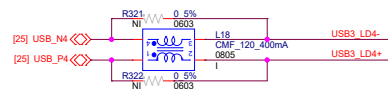
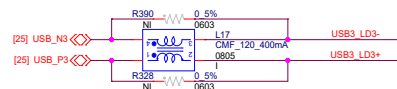


REAR USB3.0X2



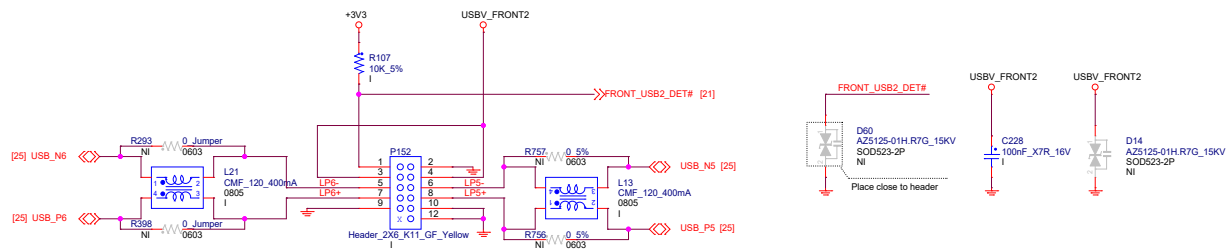
Remove the CMC/0ohm co-lay solution
for USB3 signals in SIT phase

ESD suppressor

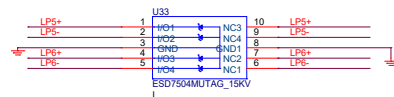


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Card Reader USB Port



ESD suppressor

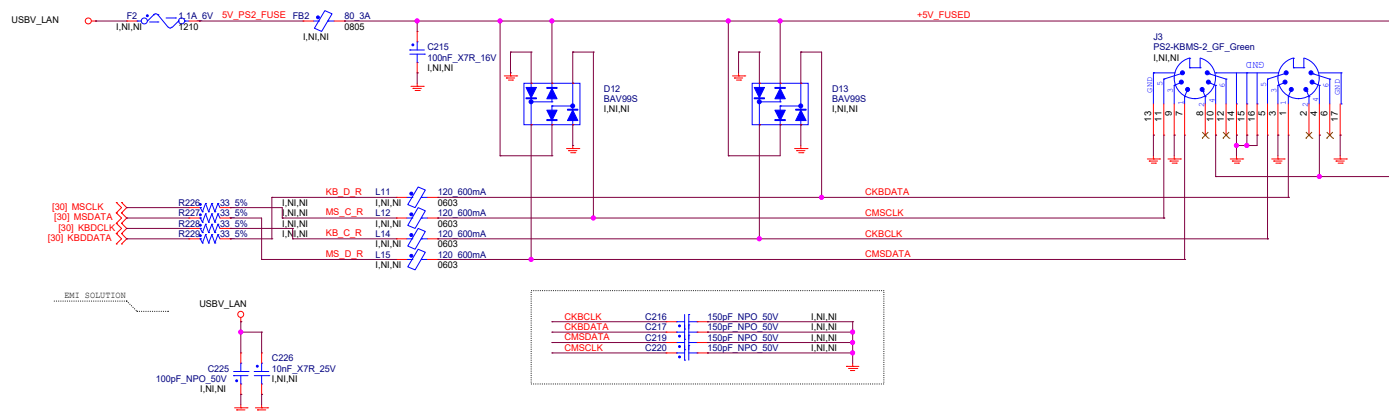


BOM DISTRIBUTION RULE

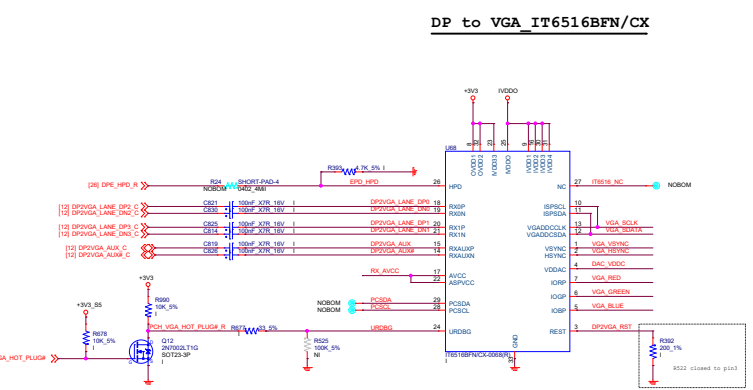
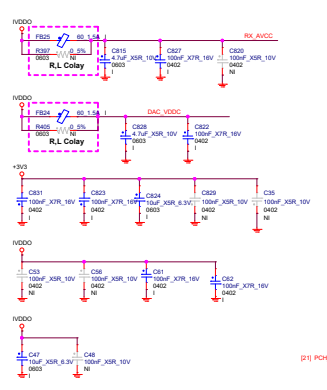
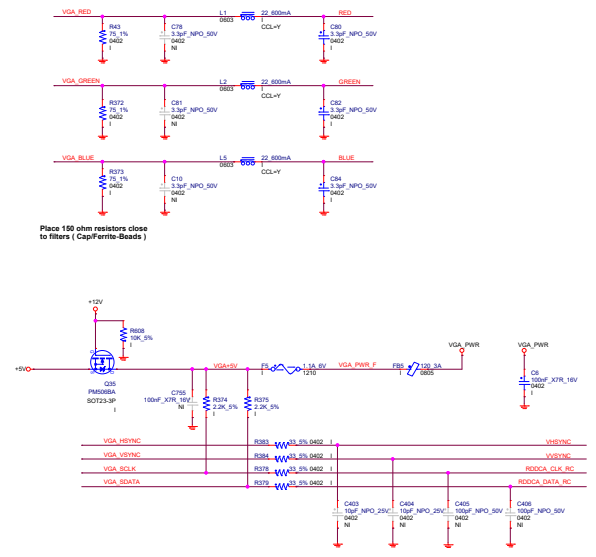
QT,SMB&Consumer,Think M70e
(BOM, BOM, BOM)

KEYBOARD / MOUSE

The +5V_FUSED power trace width must be 40 mils or greater

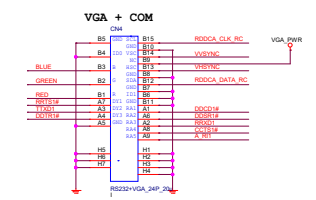


VGA

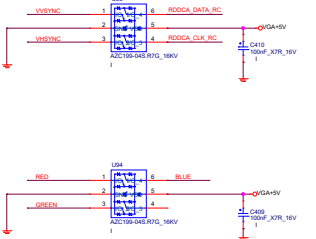


Pin24 (HPO_R)	Pin28 (HPO)	VGA Device
HDR	HDR	Plug In or Un-Plug
LOW	LOW	Plug In
LOW	LOW	Un-Plug

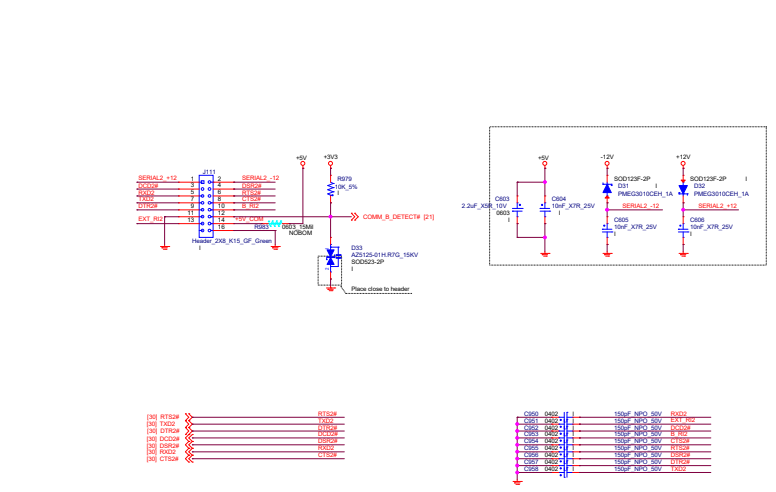
DP to VGA IT6516BFN/CX



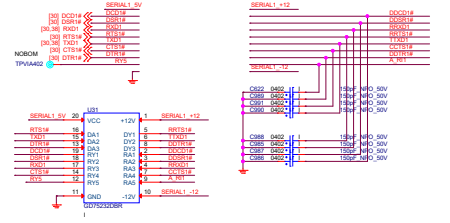
ESD pads are as close as possible to I/O connector pins. capacitor pads are as close as possible to the ESD diode.



COM2 on Header

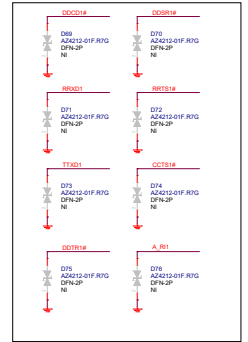
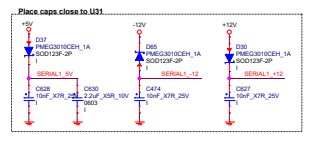
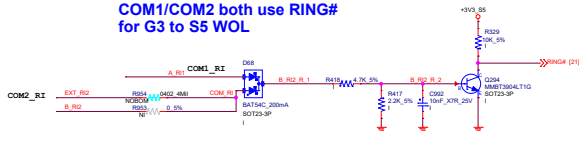


COM1 on board



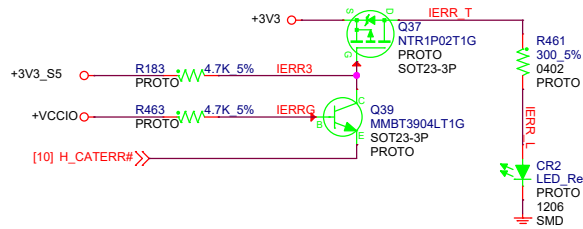
SIT change U31 from SN75185DBR to GD75232DBR

COM1/COM2 both use RING# for G3 to S5 WOL

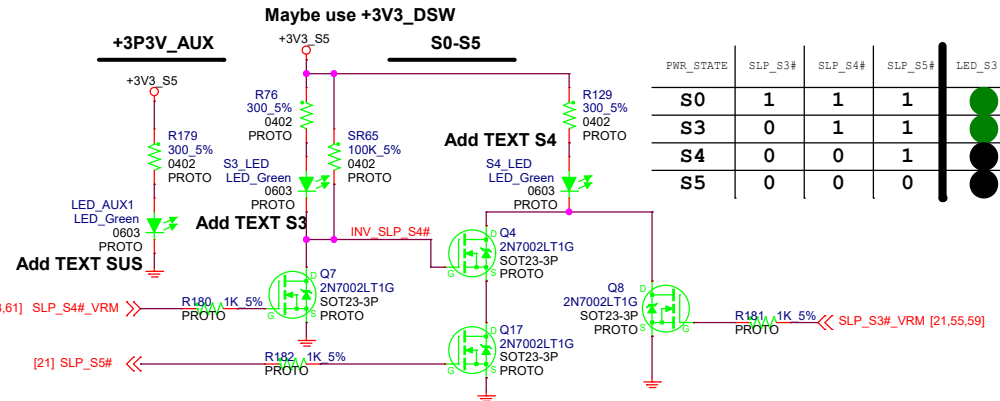


EMC Request

PCA LED

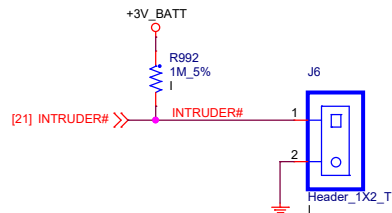


CATERR#

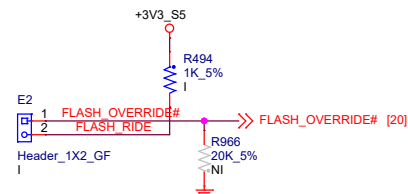


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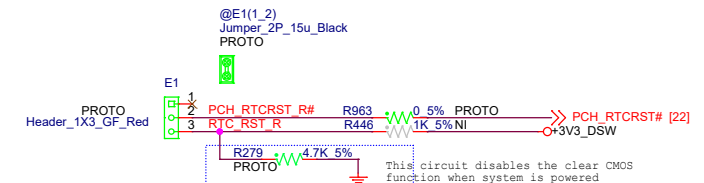
Case Open



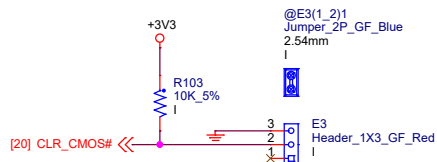
FLASH OVERRIDE(ME Disable)



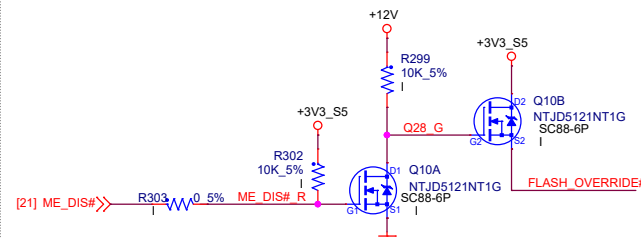
CLEAR CMOS HW



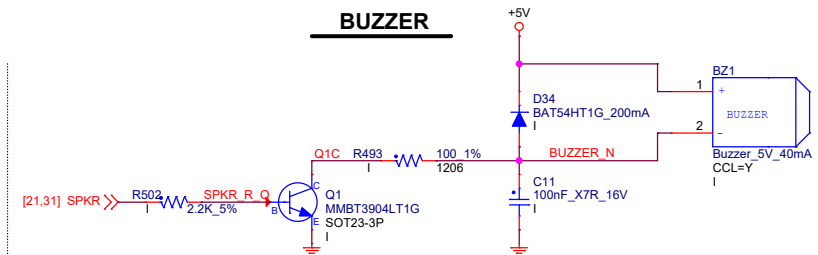
CLR CMOS



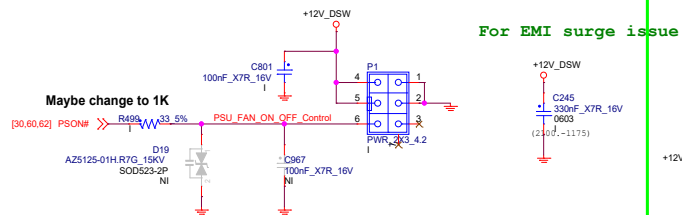
SW FLASH OVERRIDE



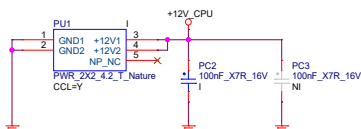
BUZZER



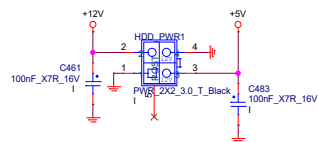
Power Input Connector



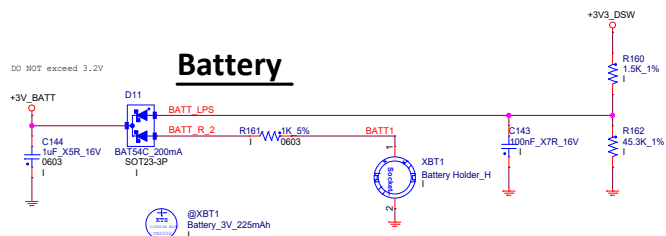
CPU POWER



SATA POWER

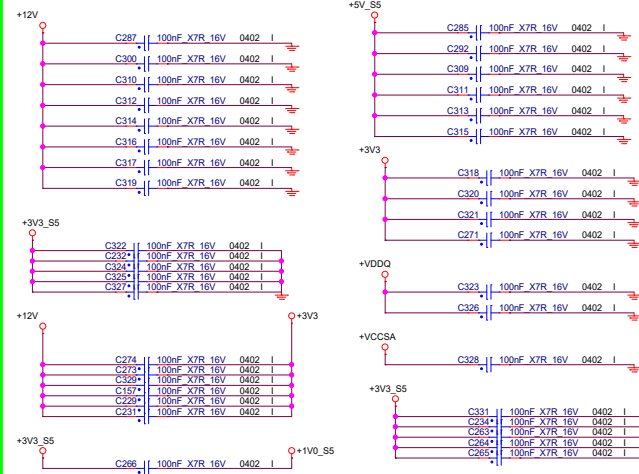


Battery

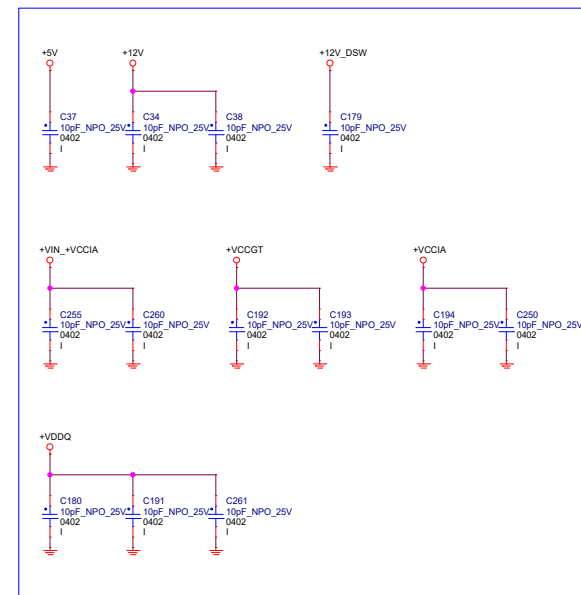


FXN EMI SUGGESTED PLACEMENT

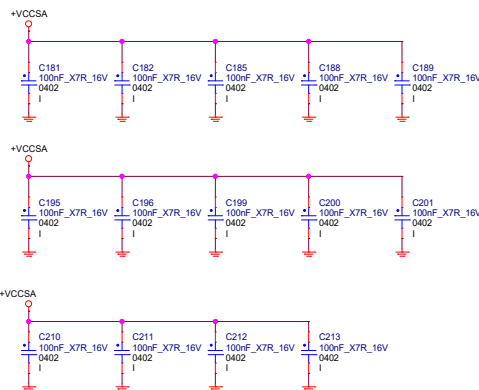
FXN EMI SUGGESTED PLACEMENT



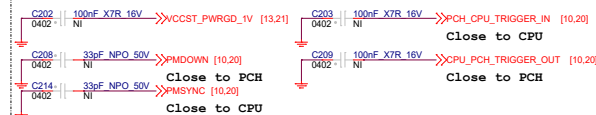
Need follow RF team suggest location

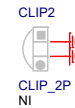
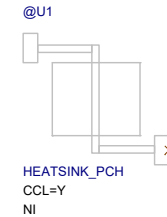
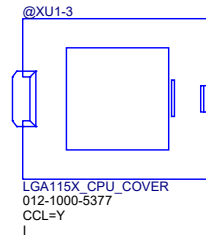
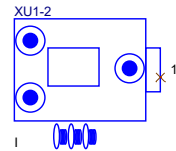
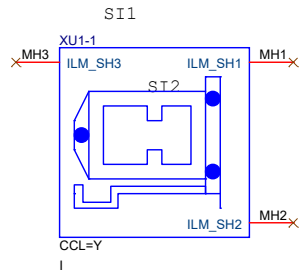
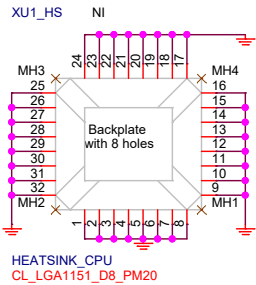


HSIO Stitching Caps

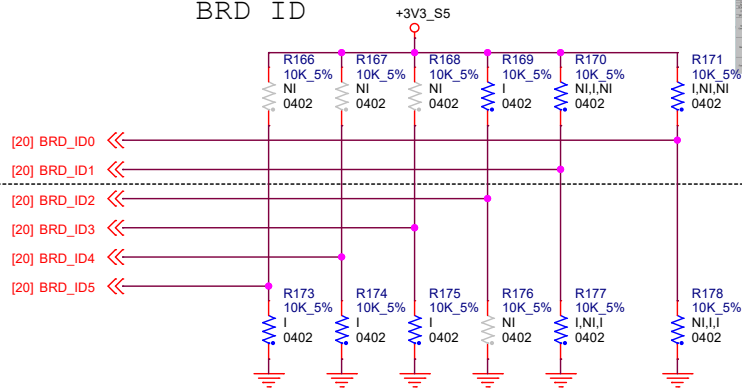
CPU STICHING CAP for PEGx16 [Note 1](#)

Note3

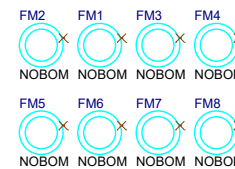
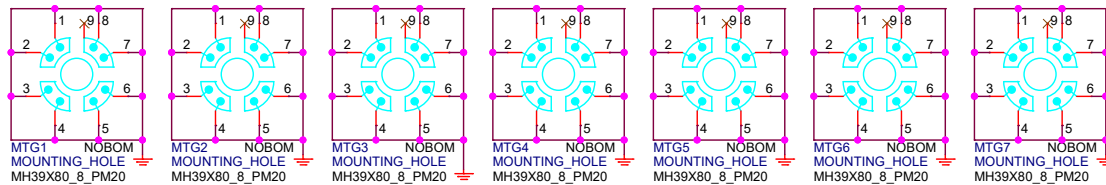
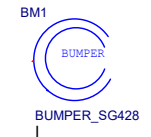




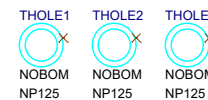
BRD ID



SKU	BRD_ID2	BRD_ID1	BRD_ID0
QT	0	0	1
SMB&Consumer	0	1	0
M70e	0	0	0
QT	1	0	1
SMB&Consumer	1	1	0
M70e	1	0	0



DFT Tooling Hole



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Foxconn WuHan
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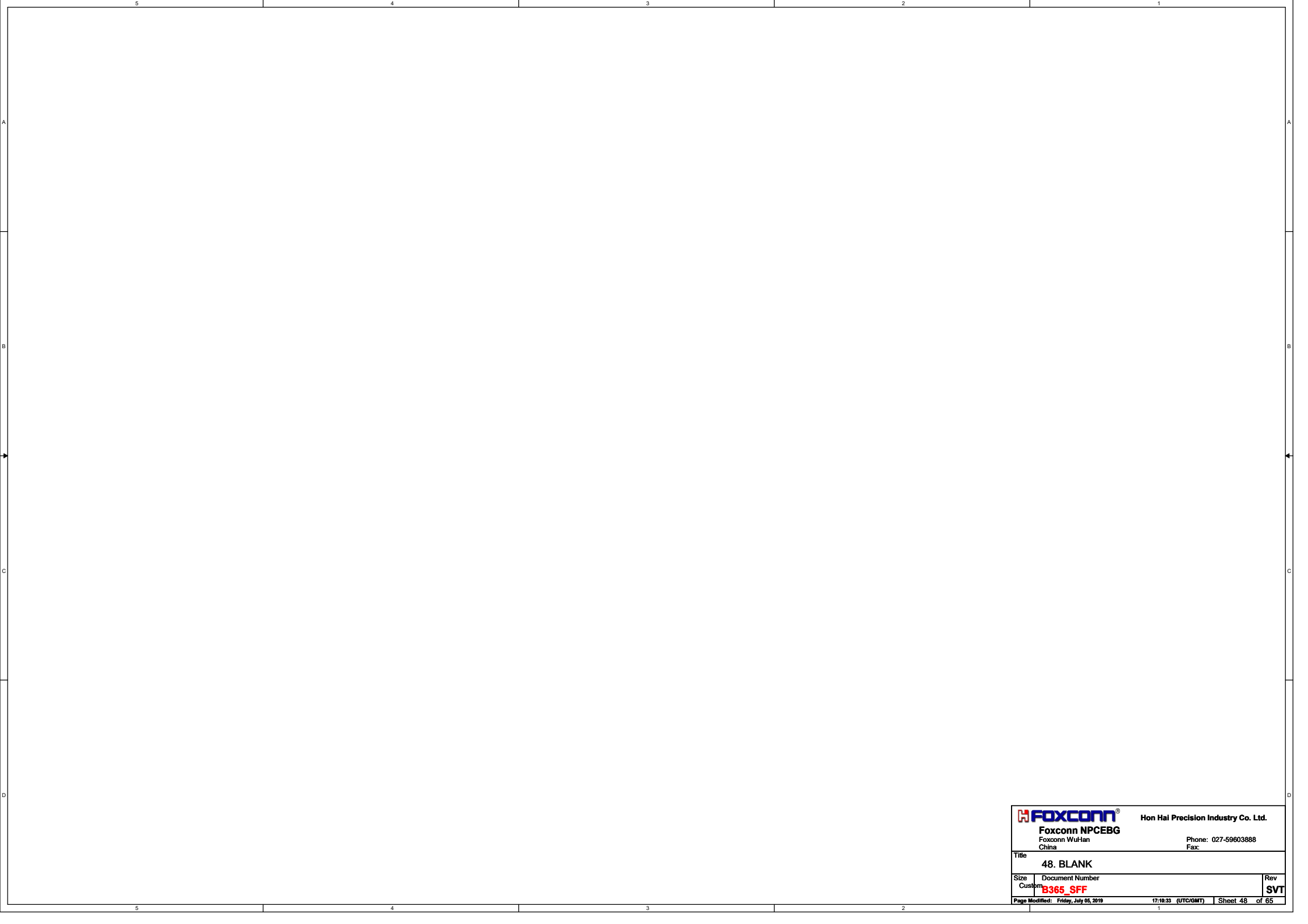
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47.MECHANICAL PARTS

Size
B


Document Number
B365_SFF

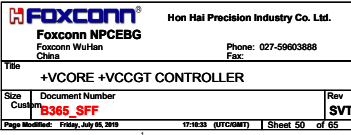
Rev
SVT

Page Modified: Friday, July 05, 2019 17:10:33 (UTC/GMT) Sheet 47 of 65

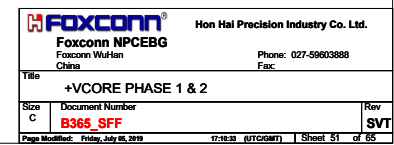


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A					
B					
C					
D					
	1	2	3	4	5

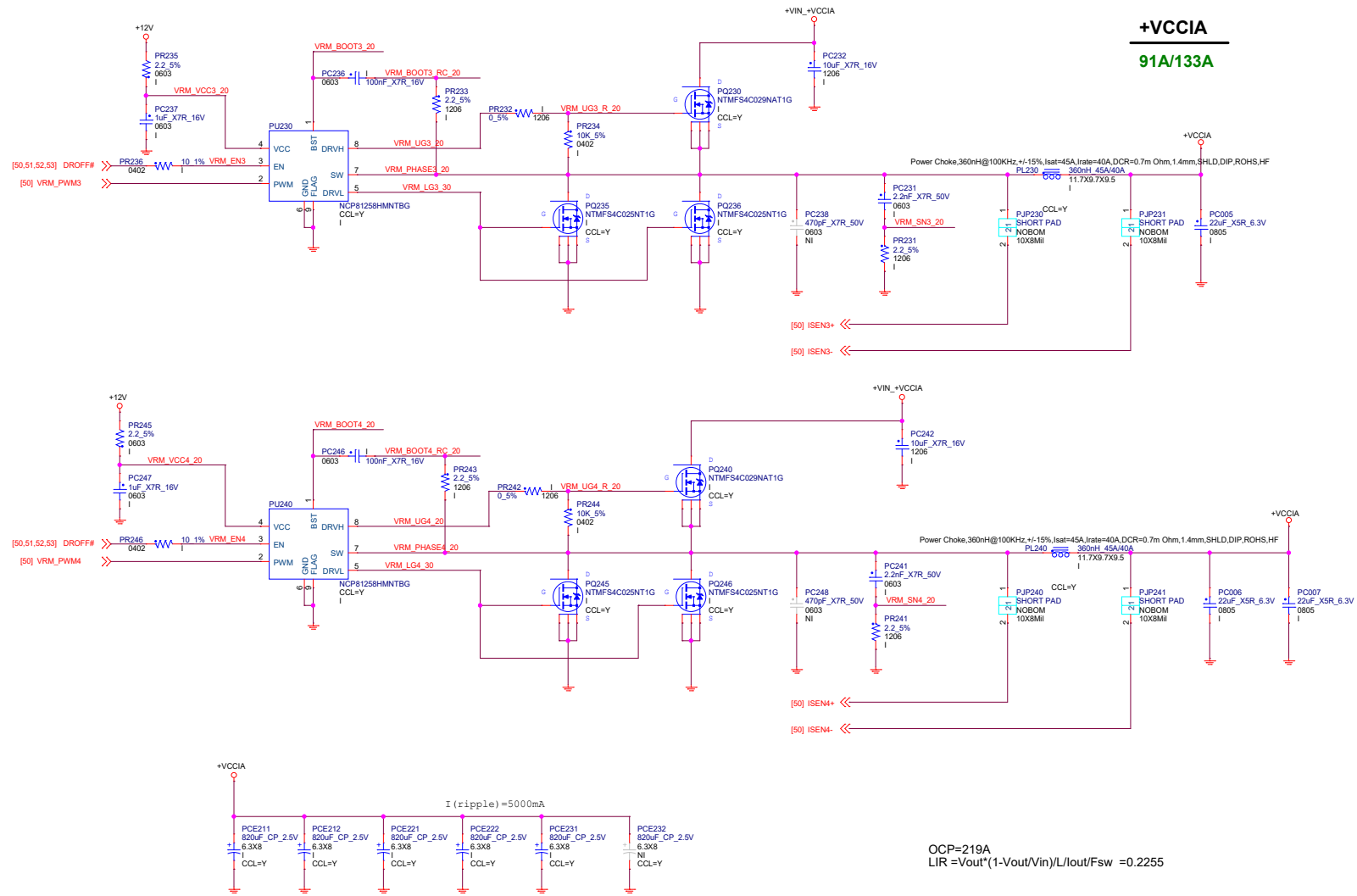
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Foxconn NPCEBG		Phone: 027-59603888	
Foxconn WuHan		Fax:	
China			
Title			
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Size	Document Number		Rev
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Page Modified: Friday, July 05, 2019		17:10:33 (UTC/GMT)	Sheet 49 of 65



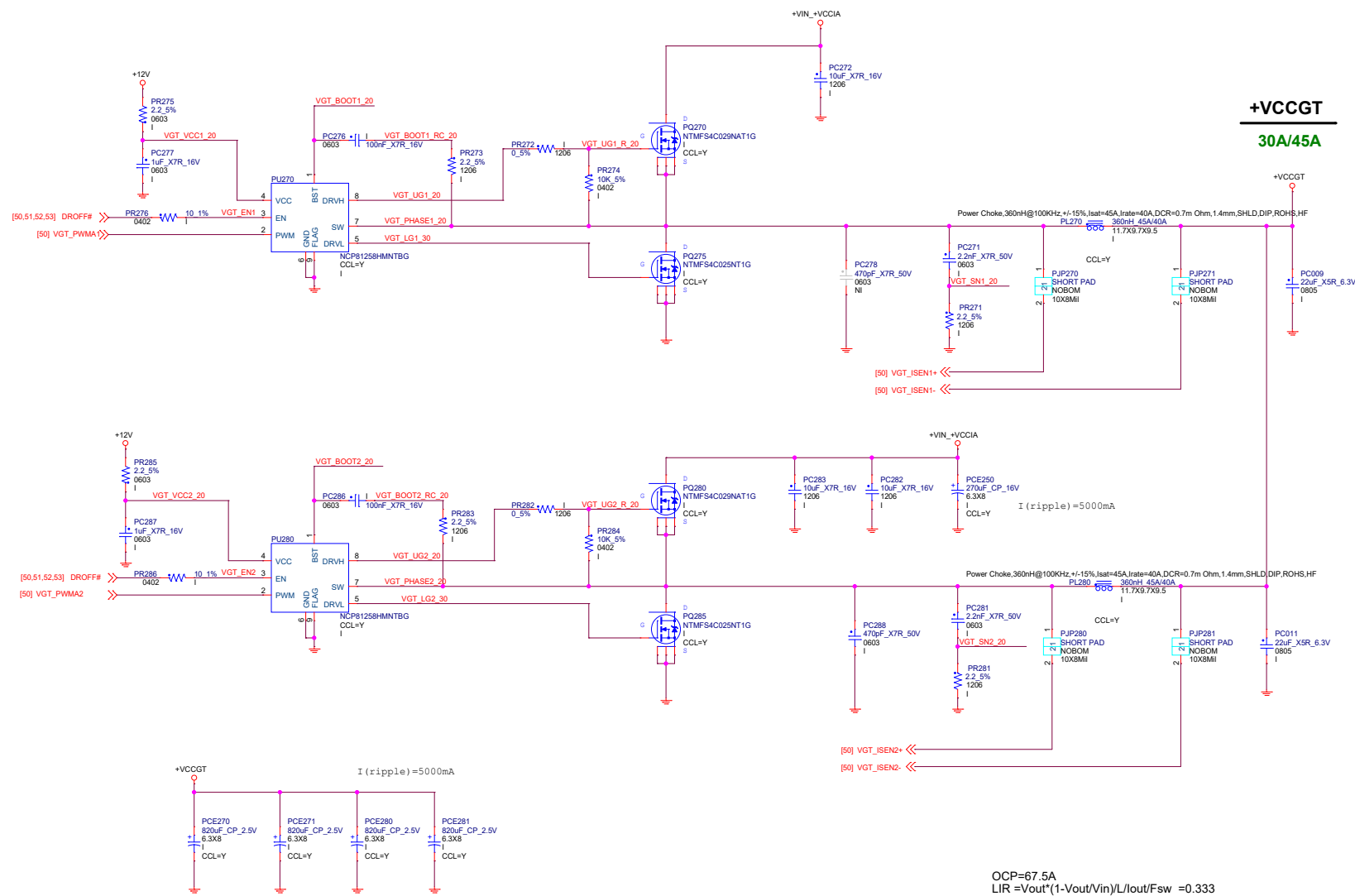
VCORE PHASE1~2



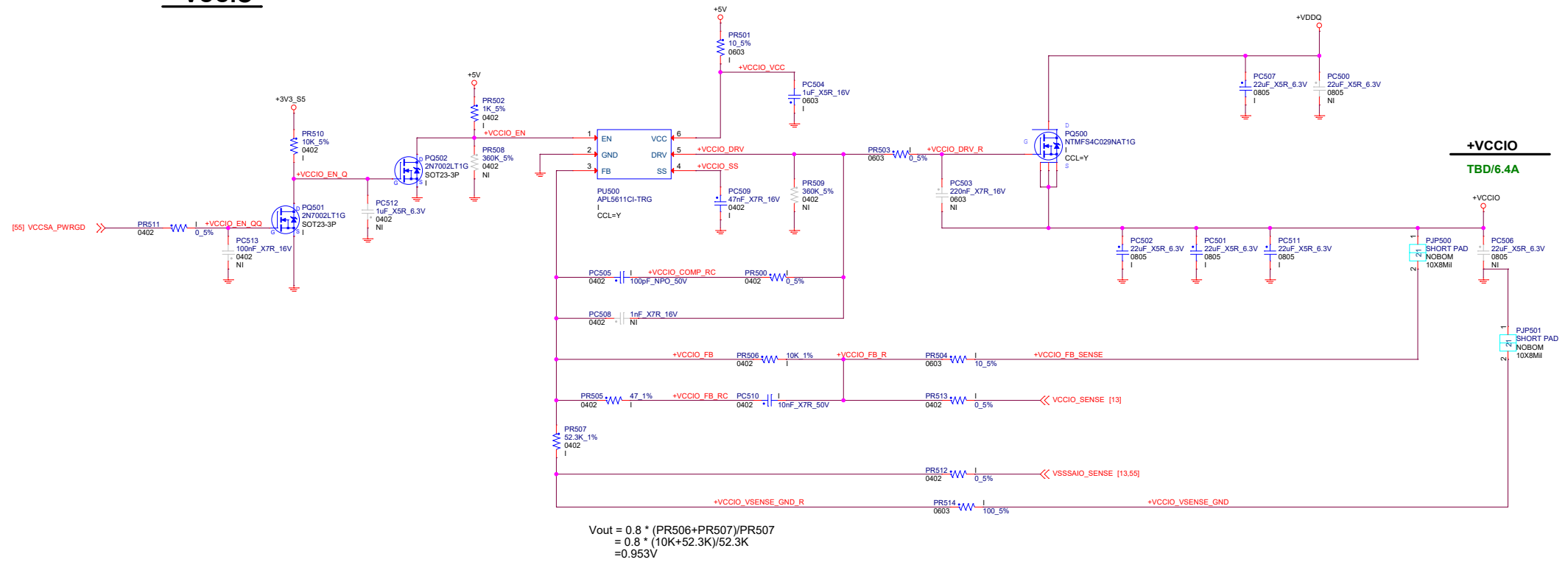
VCORE PHASE3~4



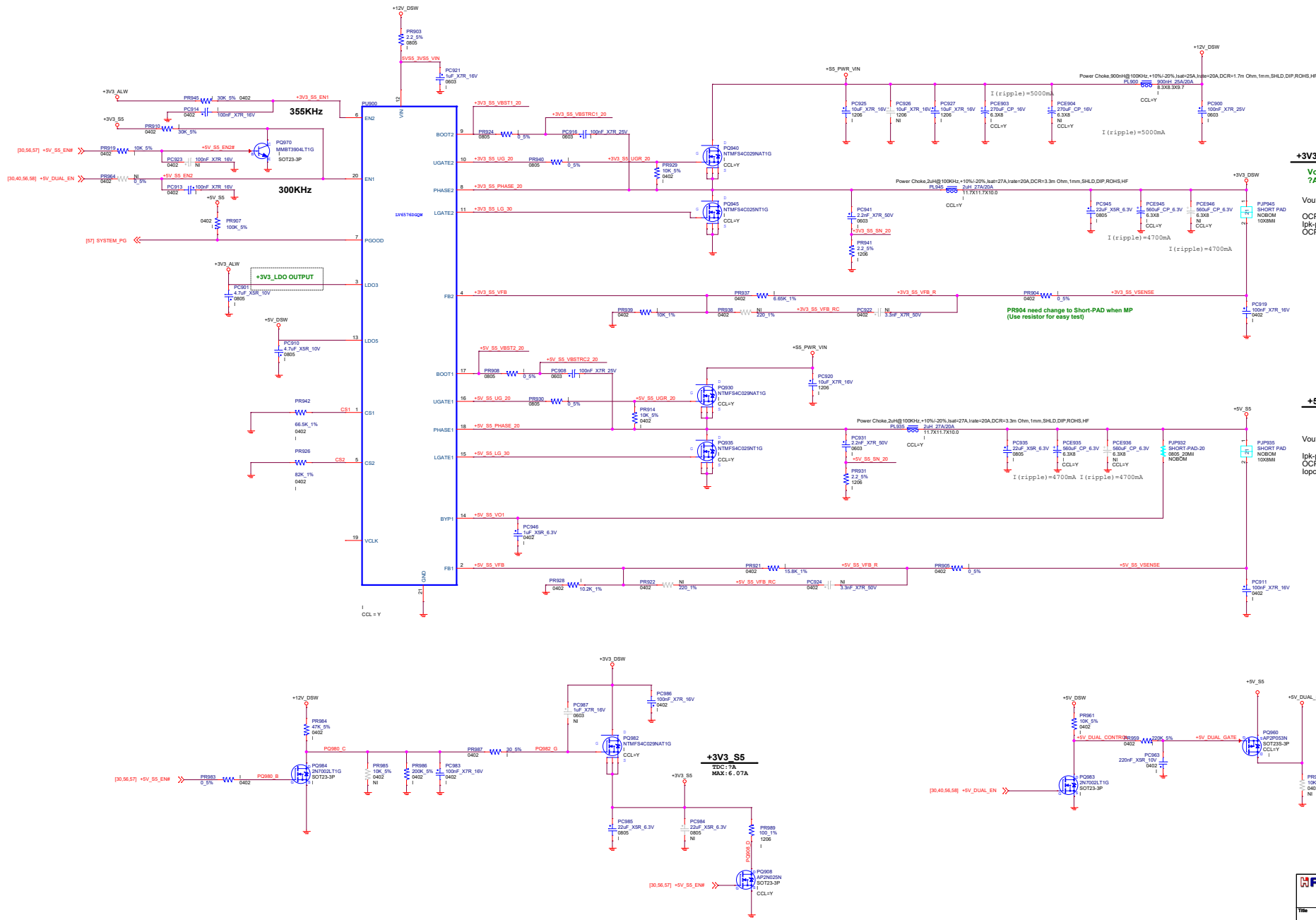
VCCGT PHASE1~2



+VCCIO



$$\begin{aligned} V_{out} &= 0.8 * (PR506+PR507)/PR507 \\ &= 0.8 * (10K+52.3K)/52.3K \\ &= 0.953V \end{aligned}$$



+3V3_DSW

Vout= 3.3V
7A/15.03A

Vout = 2 * (1+PR937/PR939)
= 3.3V
OCP set point: Rcs2
l_{pk-pk} = (12-3.3) * 3.3 / 12 / 355 = 3.37A
OCP = (Rcs * l_{cs} / 8 / R_{dson} + l_{pk-pk} / 2)
= 27.25A

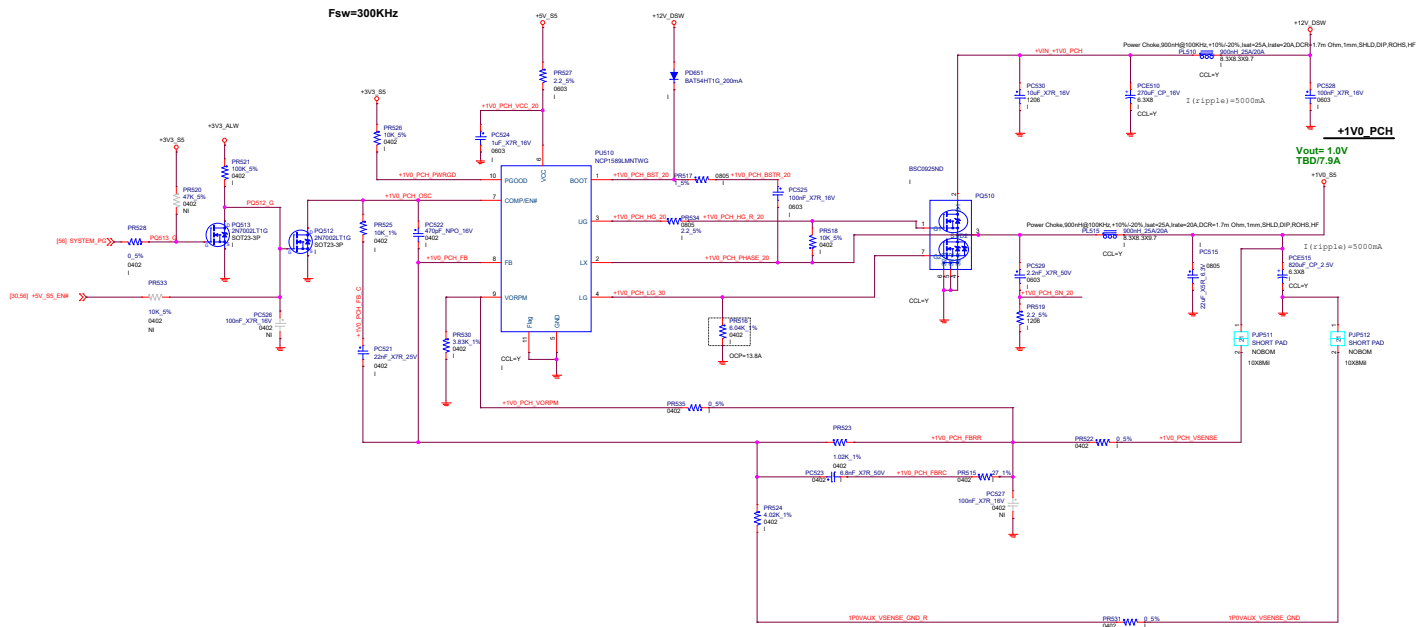
+5V_SS

Vout= 5V
7A/12.7A

Vout = 2 * (1+PR921/PR928)
= 5.098V
l_{pk-pk1} = (12-5) * 5 / 12 / 300 = 4.86A
OCP set point: Rcs1
l_{opc} = R_{ocset} * l_{ocset} / 8 / R_{dson} + l_{pk-pk} / 2
= 23.16A

+5V_DUAL_S3

ZDC1: 7A
MAX: 0.3A




$$V_{out} = 0.8 \cdot (1 + PR523/PR524) = 1.00V$$

$$I_{pk-pk} = (12 \cdot 1)^2 / 12 / 0.9 / 300 = 3.34A$$

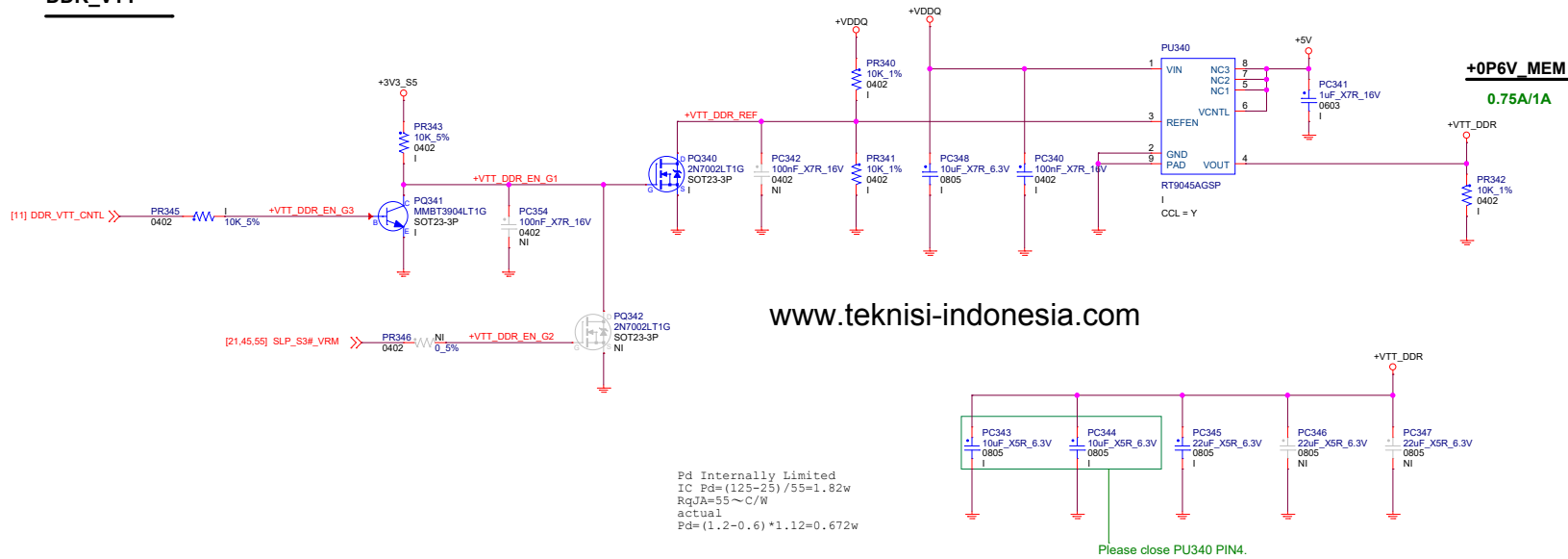
$$I_{DC} = (R_{load} + I_{load}) / R_{load} + I_{pk-pk} / 2 = 13.8A$$

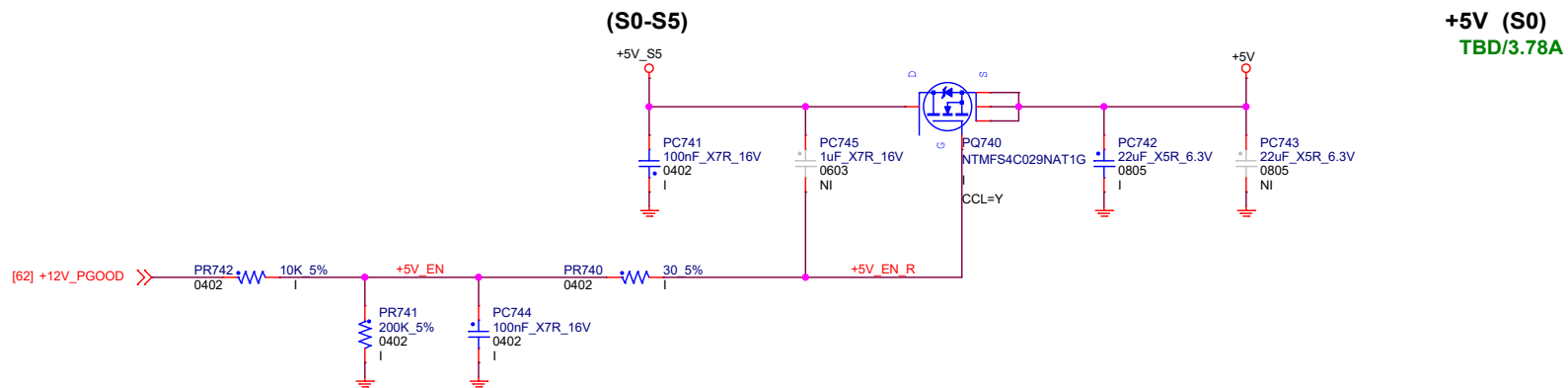
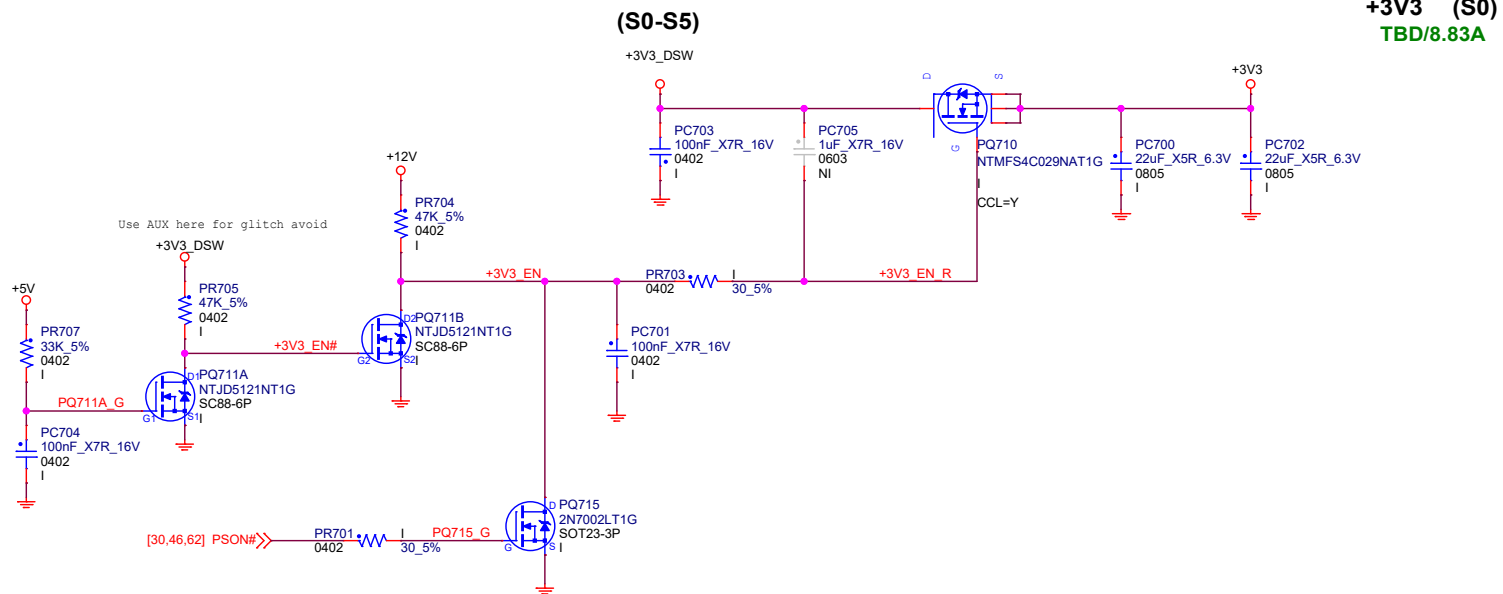
Note: net-name:+VDDQ

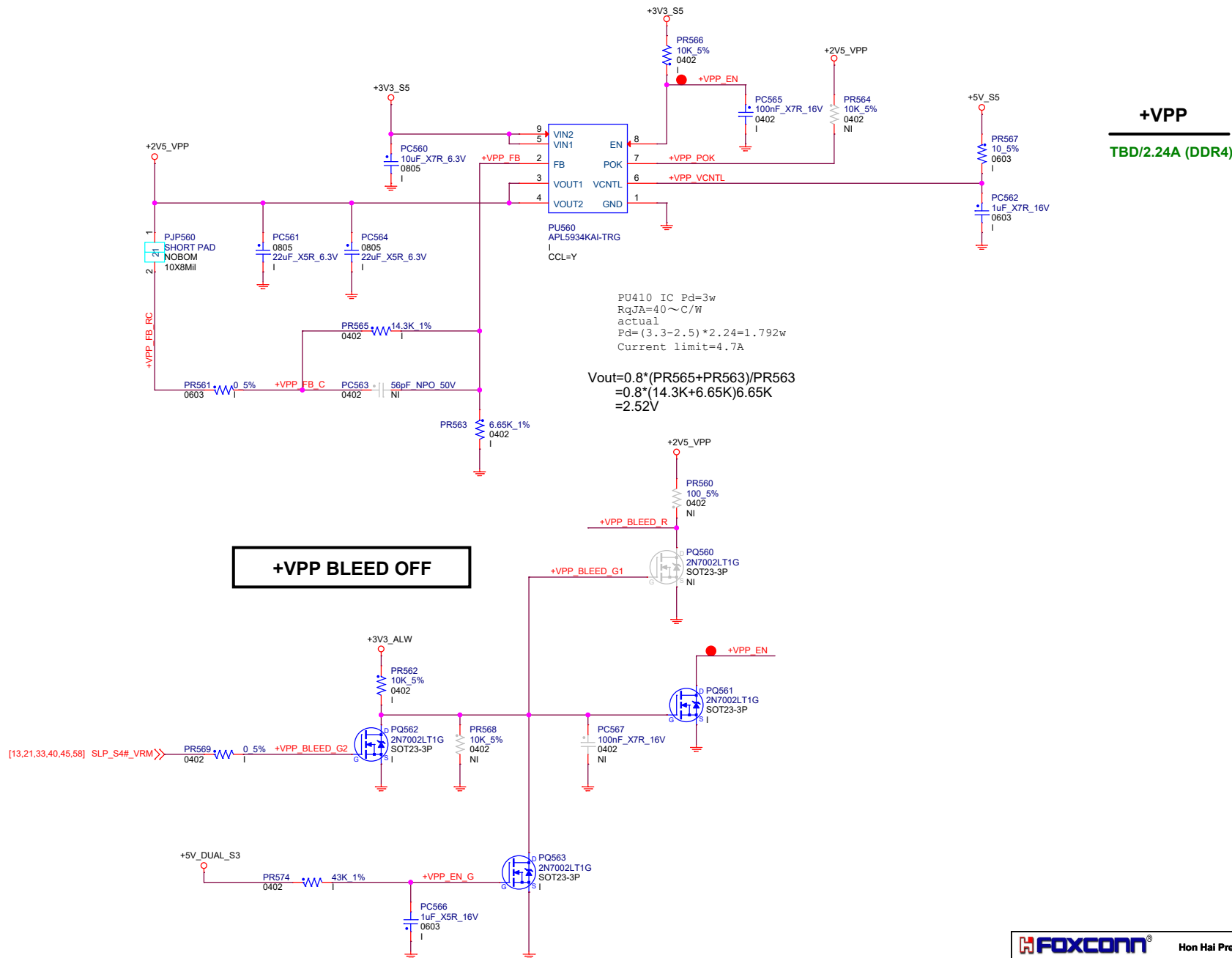


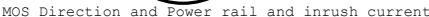
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Size Custom	Document Number <div style="border: 1px solid black; padding: 5px; text-align: center;"> R366 SFF </div>		Rev SVT
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DDR_VTT



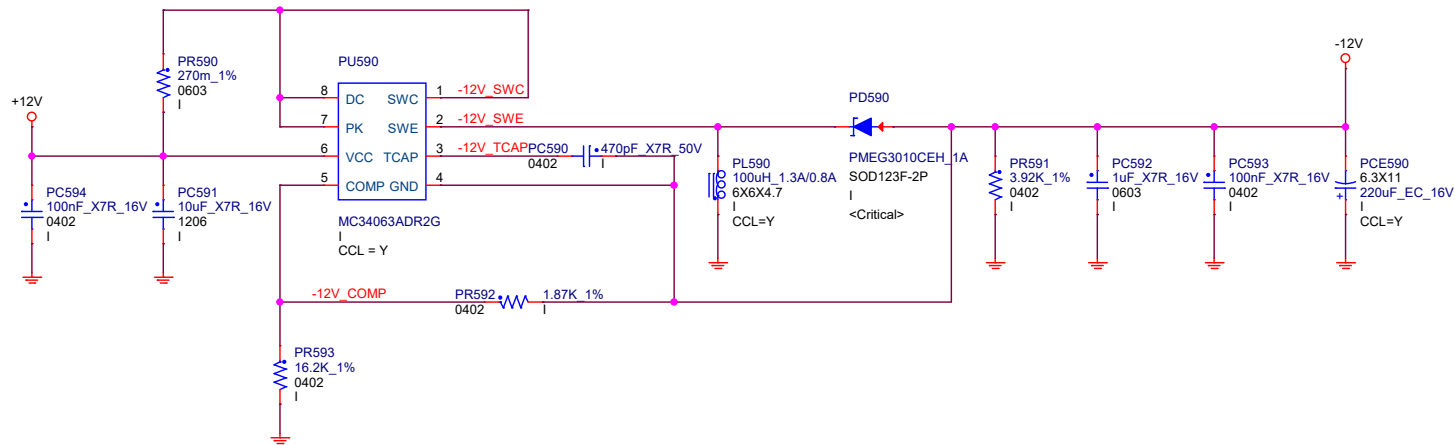






-12V

**Vout= -12V
TBD/0.019A**



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Foxconn NPCEBG		Foxconn WuHan China	
Title		-12V	
Size B	Document Number	Rev	SVT
B365_SFF			
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SDV to SIT change List(EE Part)

Schematic Information Update

Page1

- Update "PROJECT INFORMATION"
- * PHASE: SIT (VER:0.3) 2019/06/19
- * BOM : Waiting

ALL Page

- Title Block
- * Rev : SIT

Schematic Change

- PCB Change
 - * Keep SDV PCB
- Schematics & BOM Change
 - * Remove 2n source part of USB Power SW without discharge circuit APL3551DBI-TRG
 - * "NI" USB Discharge Circuit Q305,Q304,Q303,Q302,Q13,R492,R382
 - * Change RS232 Driver U31 from SN75185DBR to GD75232DBR
 - * Change B365 PCH P/N from 210134V00-187-G to 210134V00-187-H
 - * Change LPT Termination U3 to URCZ1284G-02-SQ8-R
 - * Change AJ1,2,3 and SW1,2 Package item to DIP
 - * "NI" C247 (IUSB PWRSW 22uF)
 - * "NI" R131 (SATALED PU)
 -
 - * C160,C161 change to 27pF (for 24MHz)
 - * add C112,C113 (2.2uF for VREFCA)
 - * add 3V3 discharge circuit install SQ3,SR107
 - * change AR49,AR51 to 56_1% Ohm for front combo jack out

Layout Change

- * No Change

SIT to SVT change List(EE Part)

- * Remove PROTO Parts from BOM
- * Change PCB Ver to V1.0
- * Change XDP footprint for MP
- * Change BIOS ROM to SMD
- * change AJ1,2,3 and SW1,2 to SMD

SDV phase change List(DC Part)

20190507

- 1 } change PR523 value to 1.02k for +1v0_PCH
- 2 } change PR524 value to 4.02k for +1v0_PCH
- 3 } change PR516 value to 6.04k for +1v0_PCH
- 4 } remove +1V8_S5 part

20190508

- 1 } PL605 change from MMD-06CZ-R68M-V1-B3 to WSSPG0603-R68M-AG of MAGIC for VCCSA

20190514

- 1 } PCE210,PCE220,PCE230,PCE250,PCE470,PCE510,PCE903,PCE904 change from APSF160ETD271MH08S to APSG160ETD271MF08J for automation

20190517

- 1 } PCE605 change from I to NI for cost down